# 20-Bit, Low-Power Digital-to-Analog Converter

**Check for Samples: DAC1220**

## FEATURES

- **20-Bit Monotonicity Ensured Over –40°C to +85°C**
- **Low Power: 2.5mW**
- **Voltage Output**
- **Settling Time: 2ms to 0.012%**
- **Maximum Linearity Error: ±0.0015%**
- **On-Chip Calibration**

## APPLICATIONS

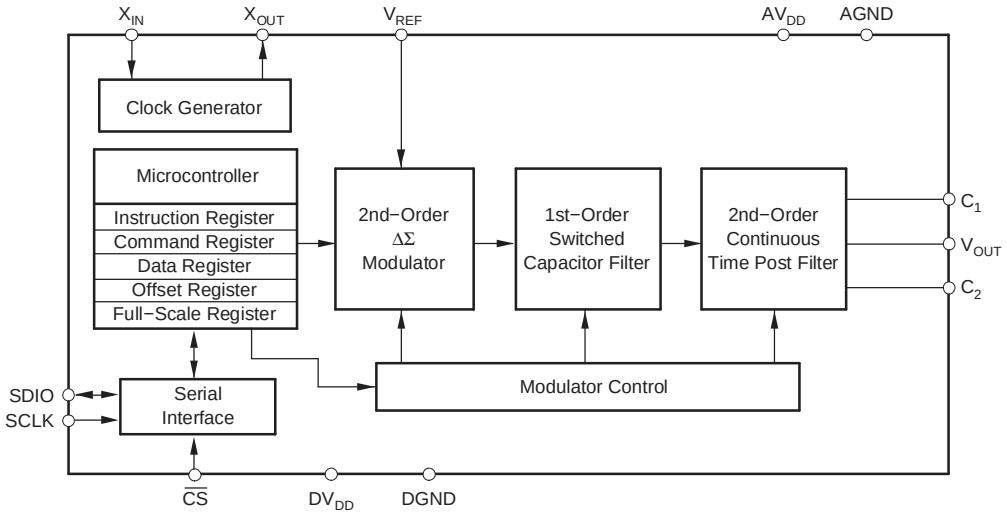
- **Process Control**
- **ATE Pin Electronics**
- **Closed-Loop Servo Control**
- **Smart Transmitters**
- **Portable Instruments**

## DESCRIPTION

The DAC1220 is a 20-bit digital-to-analog (D/A) converter offering 20-bit monotonic performance over the specified temperature range. It utilizes delta-sigma technology to achieve inherently linear performance in a small package at very low power. The resolution of the device can be programmed to 20 bits for Full-Scale, settling to 0.003% within 15ms typical, or 16 bits for Full-Scale, settling to 0.012% within 2ms max. The output range is two times the external reference voltage. On-chip calibration circuitry dramatically reduces low offset and gain errors.

The DAC1220 features a synchronous serial interface; in single-converter applications, the serial interface can be accomplished with just two wires, allowing low-cost isolation. For multiple converters, a $\overline{CS}$ signal allows for selection of the appropriate D/A converter.

The DAC1220 has been designed for closed-loop control applications in the industrial process control market and high-resolution applications in the test and measurement market. It is also ideal for remote applications, battery-powered instruments, and isolated systems. The DAC1220 is available in an SSOP-16 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | DAC1220 | UNIT |
|---|---|---|
| $AV_{DD}$ to $DV_{DD}$ | ±0.3 | V |
| $AV_{DD}$ to AGND | –0.3 to +6 | V |
| $DV_{DD}$ to DGND | –0.3 to +6 | V |
| AGND to DGND | ±0.3 | V |
| $V_{REF}$ voltage to AGND | +2.0 to +3.0 | V |
| Digital input voltage to DGND | –0.3 to $DV_{DD}$ + 0.3 | V |
| Digital output voltage to DGND | –0.3 to $DV_{DD}$ + 0.3 | V |
| Package power dissipation | $(T_J max - T_A) / \theta_{JA}$ | W |
| Maximum junction temperature ($T_J$max) | +150 | °C |
| Thermal resistance, $\theta_{JA}$ SSOP-16 | 200 | °C/W |
| Lead temperature (soldering, 10s) | +300 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

All specifications at $T_{MIN}$ to $T_{MAX}$, $AV_{DD}$ = $DV_{DD}$ = +5V, $f_{XIN}$ = 2.5MHz, $V_{REF}$ = +2.5V, and 16-bit mode, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC1220E | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **ACCURACY** | | | | | |
| Monotonicity | | 16 | | | Bits |
| Monotonicity | 20-bit mode | 20 | | | Bits |
| Linearity error | | | | ±15(1) | ppm of FSR |
| Unipolar offset error and gain error(2) | | | | ±60 | ppm of FSR |
| Unipolar offset error drift(3) | | | 1 | | ppm/°C |
| Bipolar zero offset error(2) | $V_{OUT}$ = $V_{REF}$ | | ±15 | | ppm of FSR |
| Bipolar zero offset drift(3) | | | 1 | | ppm/°C |
| Gain error(2) | | | | ±150 | ppm of FSR |
| Gain error drift(3) | | | 2 | | ppm/°C |
| Power-supply rejection ratio (PSRR) | at DC, dB = –20log($\Delta V_{OUT}/\Delta V_{DD}$) | | 60 | | dB |
| **ANALOG OUTPUT** | | | | | |
| Output voltage(4) | | 0 | | 2 × $V_{REF}$ | V |
| Output current | | | | 0.5 | mA |
| Capacitive load | | | 500 | | pF |
| Short-circuit current | | | ±20 | | mA |
| Short-circuit duration | GND or $V_{DD}$ | | Indefinite | | |
| **DYNAMIC PERFORMANCE** | | | | | |
| Settling time(5) | To ±0.012% | | 1.8 | 2 | ms |
| | 20-bit mode, to ±0.003% | | 15 | | ms |
| Output noise voltage | 0.1Hz to 10Hz | | 1 | | $\mu V_{RMS}$ |
| **REFERENCE INPUT** | | | | | |
| Input voltage | | 2.25 | 2.5 | 2.75 | V |
| Input impedance | | | 100 | | kΩ |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic family | | TTL-compatible CMOS | | | |
| Logic levels (all except $X_{IN}$) | | | | | |
| $V_{IH}$ | | 2.0 | | $DV_{DD}$ + 0.3 | V |
| $V_{IL}$ | | –0.3 | | 0.8 | V |
| $V_{OH}$ | $I_{OH}$ = –0.8mA | 3.6 | | | V |
| $V_{OL}$ | $I_{OL}$ = 1.6mA | | | 0.4 | V |
| Input-leakage current | | | | ±10 | µA |
| $X_{IN}$ frequency range ($f_{XIN}$) | | 0.5 | | 2.5 | MHz |
| Data format | User-programmable | Offset binary two's complement or straight binary | | | |
| **POWER-SUPPLY REQUIREMENTS** | | | | | |
| Power-supply voltage | | 4.75 | | 5.25 | V |
| Supply current | | | | | |
| Analog current | | | 360 | | µA |
| Digital current | | | 140 | | µA |
| Analog current | 20-bit mode | | 460 | | µA |

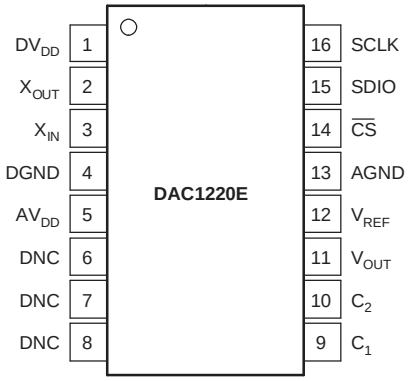
(1) Valid from AGND + 20mV to $AV_{DD}$ – 20mV.
(2) Applies after calibration.
(3) Recalibration can remove these errors.
(4) Ideal output voltage; does not take into account gain and offset error.
(5) Valid from AGND + 20mV to $AV_{DD}$ – 20mV. Outside of this range, settling time can be twice the value indicated. For 16-bit mode, $C_1$ = 2.2nF, $C_2$ = 0.22nF; for 20-bit mode, $C_1$ = 10nF, $C_2$ = 3.3nF.

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_{MIN}$ to $T_{MAX}$, $AV_{DD}$ = $DV_{DD}$ = +5V, $f_{XIN}$ = 2.5MHz, $V_{REF}$ = +2.5V, and 16-bit mode, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC1220E | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **POWER-SUPPLY REQUIREMENTS, *continued*** | | | | | |
| Digital current | 20-bit mode | | 140 | | µA |
| Power dissipation | | | 2.5 | 3.5 | mW |
| | 20-bit mode | | 3.0 | | mW |
| | Sleep mode | | 0.45 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified performance | | –40 | | +85 | °C |

## DEVICE INFORMATION




### PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $DV_{DD}$ | Digital supply, +5V nominal |
| 2 | $X_{OUT}$ | System clock output (for crystal) |
| 3 | $X_{IN}$ | System clock input |
| 4 | DGND | Digital ground |
| 5 | $AV_{DD}$ | Analog supply, +5V nominal |
| 6 | DNC | Do not connect |
| 7 | DNC | Do not connect |
| 8 | DNC | Do not connect |
| 9 | $C_1$ | Filter capacitor (see text) |
| 10 | $C_2$ | Filter capacitor (see text) |
| 11 | $V_{OUT}$ | Analog output voltage |
| 12 | $V_{REF}$ | Reference input |
| 13 | AGND | Analog ground |
| 14 | $\overline{CS}$ | Chip-select input |
| 15 | SDIO | Serial data input/output |
| 16 | SCLK | Clock input for serial data transfer |

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $AV_{DD}$ = $DV_{DD}$ = +5.0V, $f_{XIN}$ = 2.5MHz, $V_{REF}$ = 2.5V, $C_1$ = 2.2nF, and calibrated mode, unless otherwise specified.

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

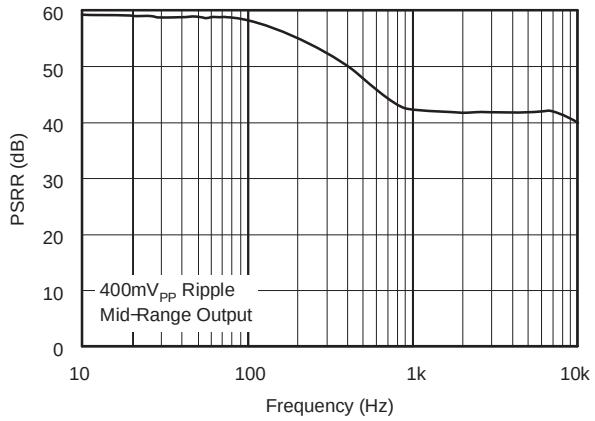



**Figure 1.**

**LARGE-SIGNAL SETTLING TIME**

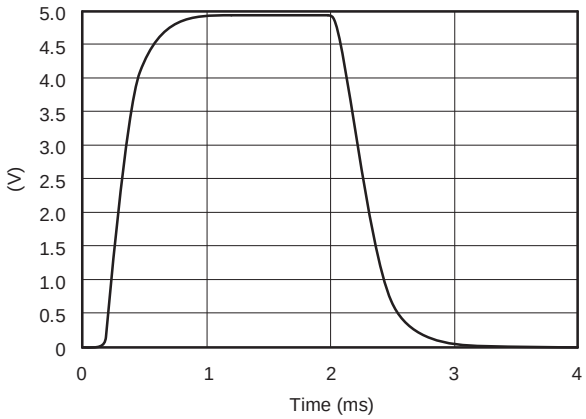



**Figure 2.**

**OUTPUT NOISE VOLTAGE vs FREQUENCY**

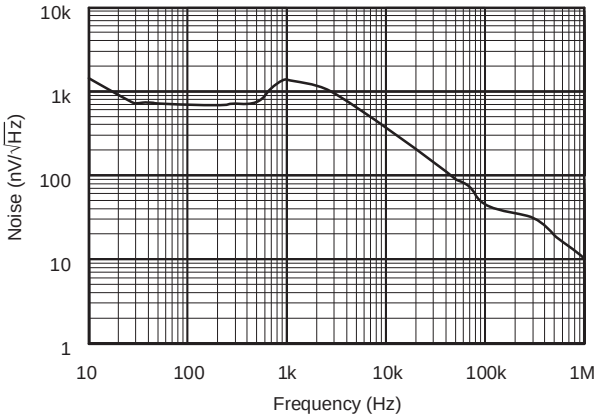



**Figure 3.**

**LINEARITY ERROR vs CODE**

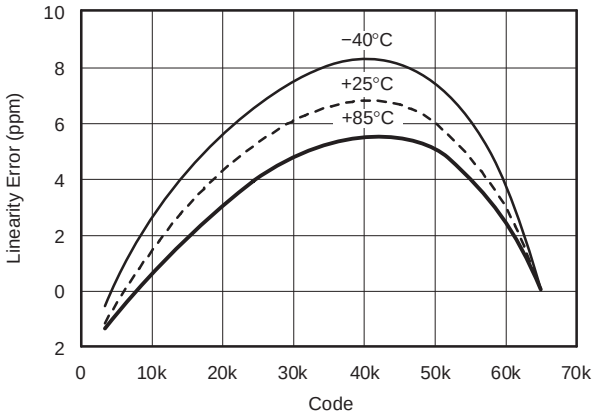



**Figure 4.**

## THEORY OF OPERATION

The DAC1220 is a monolithic 20-bit delta-sigma (ΔΣ) digital-to-analog converter (DAC) designed for applications requiring extremely high precision. The delta-sigma topology used in the DAC1220 ensures 20-bit monotonicity over the industrial temperature range. The DAC1220 can also be operated in 16-bit mode, which gives a faster settling time at the expense of higher noise.

The core of the DAC1220 consists of an interpolation filter and a second-order delta-sigma modulator. The output of the modulator is passed to a first-order switched-capacitor filter in series with a second-order continuous-time filter, which generates the output voltage.

To increase settling time, the DAC1220 can adjust its filter cutoff frequency when it detects a voltage output step of greater than approximately 40mV. This behavior can be disabled.

An onboard self-calibration facility compensates for internal offset and gain errors. Calibration values may be stored and loaded externally if desired.

The DAC1220 can be put into a sleep mode, in which power consumption is cut by about 1/6 to approximately 0.45mW. In sleep mode, the output is disconnected.

The DAC1220 is controlled using a synchronous serial interface, using either two or three wires. The interface may be operated bidirectionally or unidirectionally; readback is optional.

### Self-Calibration System

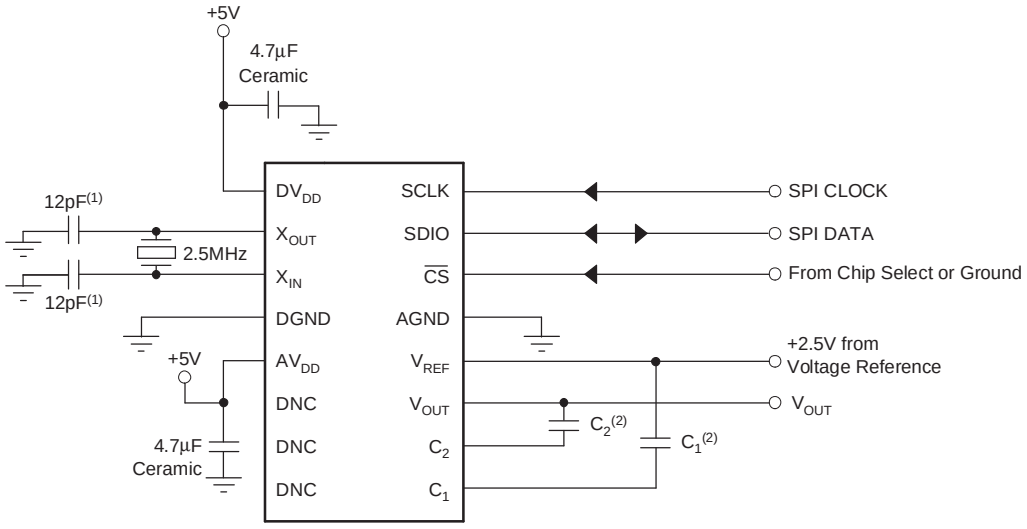
The self-calibration system of the DAC1220 measures the DAC output and calculates appropriate gain and offset calibration constants. The output changes during calibration, but can optionally be disconnected during the procedure.

Offset calibration is performed by setting the DAC output voltage to mid-scale and repeatedly comparing the DAC output to the $V_{REF}$ voltage using an auto-zeroed comparator, which is re-zeroed after every comparison. The comparator results are recorded and averaged, two's complement adjusted, and placed in the Offset Calibration Register.

Gain calibration is performed in a similar way, except that the correction is done against an internally-generated reference voltage, and the final register value is calculated differently. The Full-Scale Calibration Register result represents the gain code and is not two's complement adjusted. Changing the Gain Register value can change the range of voltages that are output for the same digital codes, centered on $V_{REF}$.

## BASIC CONNECTIONS

A schematic showing basic connections to the DAC1220 is given in Figure 5.




NOTES: (1) Depends on crystal and board layout. (2) See text for recommended values.

**Figure 5. DAC1220 Schematic**

## Output

The output voltage range is nominally 0V to 2 × $V_{REF}$. It does not go below ground. The output amplifier is not designed for heavy loads; it can drive a maximum of 0.5mA. At power-on and during sleep mode, the amplifier is disconnected, so the output is high impedance.

The output is not fully linear to the rails; maximum linearity is specified from (AGND + 20mV) to ($AV_{DD}$ – 20mV). For linearity from 0–5V, $AV_{DD}$ can be increased to 5.02V or more, and AGND can be decreased to –20mV or less. As long as the specified operating limits are observed, this will not damage the device.

## Filter Capacitors

The continuous-time output filter requires two external capacitors to operate. The recommended values of these capacitors depend on whether the DAC1220 will be operated in 16-bit or 20-bit mode, and are shown in Table 1.

**Table 1. Filter Capacitor Values**

| CAPACITOR | 16-BIT MODE | 20-BIT MODE |
|---|---|---|
| $C_1$ | 2.2nF | 10nF |
| $C_2$ | 0.22nF | 3.3nF |

The capacitors should be stable and high grade. Film types, or other capacitors designed for precision filtering, are strongly recommended. Low-quality capacitors will degrade performance significantly.

The $C_1$ and $C_2$ pins are very sensitive. It is critical to surround them with a guard ring at the reference voltage for best noise performance. See the *Layout* section for more information.

## Voltage Reference

The voltage reference input is designed for +2.5V. At this voltage, the output will range from ground to approximately 5V, as noted above.

## Digital Connections

The digital lines, except for the crystal oscillator lines, operate at TTL-compatible CMOS logic levels. They can be driven from 3.3V logic sources.

In noise-sensitive applications, it may be helpful to keep the level transition rates on the digital lines slow. Fast transitions can couple through the device to the output, causing noise. Rate limiting can be done with resistance or even an RC filter.

## Clock Oscillator

The DAC1220 has a built-in crystal oscillator at pins $X_{IN}$ and $X_{OUT}$. To use it, connect a crystal and load capacitors as shown in Figure 5.

12pF load capacitors are shown in the schematic, but the correct value depends mainly on the crystal and layout, and not on the oscillator itself. Load capacitance affects startup time, oscillation frequency, and reliability. If startup is unreliable, try lowering the capacitor values. Remember that parasitic board and pin capacitance can be a significant portion of the crystal load capacitance.

When the crystal oscillator is operating, a sinusoidal signal of relatively low amplitude will be observed at both the $X_{IN}$ and $X_{OUT}$ pins.

The typical frequency to use with the DAC1220 is 2.5MHz. Deviating too far from this may alter noise and settling time, as well as timing characteristics.

## Connecting an External Clock

An external clock signal can be connected at $X_{IN}$. A CMOS or TTL logic signal can be used. If an external clock signal is used, $X_{OUT}$ should be left unconnected.

In some cases, an RC filter on the clock line may reduce noise.

## Serial Interface

The DAC1220 can be operated from most SPI peripherals, or it can be bit-banged.

Note that if SDIO is operated bidirectionally, it may be necessary to place a pullup resistor on the line, so that the line will not be floating.

The serial clock is limited to one-tenth of the master clock frequency. For a 2.4576MHz master clock, the serial clock may be no faster than 245.76kHz. The designer should bear this in mind, as it may prevent the DAC1220 from being shared with other SPI devices or placed on an SPI bus, which may run much faster.

If the DAC1220 is placed on a shared SPI bus, the chip-select line must be controlled; otherwise, it can be grounded.

Although the SDIO line is bidirectional, it can be operated as an input only, as long as no register reads are performed. The DAC1220 can be operated without register reads, although for situations requiring high reliability, this is not recommended, since the device registers and operation cannot be directly verified.

## Power Supplies

The DAC1220 has separate analog and digital power supply connections. Both are intended to operate at +5V.

The digital supply must never exceed the analog supply by more than 300mV. If it does, the DAC1220 may be permanently damaged. The analog supply may be greater than the digital supply without damage, however.

Most designs will use a single power supply for $AV_{DD}$ and $DV_{DD}$. In these designs, the supplies ramp simultaneously, which is acceptable. In those designs that use separate sources for $AV_{DD}$ and $DV_{DD}$, the two supplies must be sequenced properly. This is easily done using a Schottky diode, as shown in Figure 6. The diode ensures that $DV_{DD}$ will not exceed $AV_{DD}$ by more than a Schottky diode drop.

## Brownouts and Power-On Reset

The DAC1220 incorporates a power-on reset (POR) circuit. The circuit will trigger as long as the power supply ramps up at 50mV/ms or faster. If the power supply ramps more slowly than this, the POR may not trigger.

The DAC1220 does not have a brownout detector. The POR circuit will not retrigger unless the supply voltages have approached ground. Because of this, if the supply falls to a low voltage, it may corrupt the logic of the DAC1220, causing it to operate erratically or to fail entirely. It may be necessary to forcibly discharge the supply, since the DAC1220 may occasionally fail to detect the SCLK reset pattern in this condition.

The SCLK reset pattern serves in place of a reset pin. See the *SCLK Reset Pattern* section for information.

## Supply Decoupling

Both supply pins should be heavily decoupled at the device for best performance. A 10µF multi-layer ceramic capacitor can be used for this, or a tantalum capacitor in parallel with a small (0.1µF) ceramic capacitor can be used. Both capacitors, particularly the ceramic capacitor, should be placed as close to the pins as possible being decoupled.

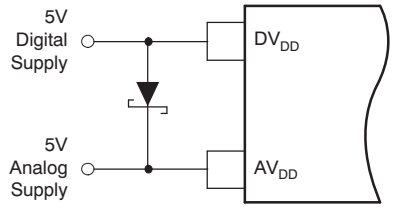



**Figure 6. Supply Sequence Protection**

## DIGITAL INTERFACE

### Timing

The serial interface is synchronous and controlled by the SCLK input. The DAC1220 latches incoming bits on the falling edge of SCLK, and shifts outgoing bits on the rising edge of SCLK. An external interface should shift outgoing bits on the rising edge of SCLK, and latch incoming bits on the falling edge of SCLK. The relevant waveforms are illustrated in the timing diagrams (see Figure 7 to Figure 11). Timing numbers are given in Table 2 through Table 4.

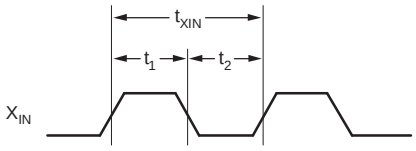



**Figure 7. $X_{IN}$ Clock Timing**

**Table 2. $X_{IN}$ Timing Characteristics**

| SYMBOL | DESCRIPTION | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| $f_{XIN}$ | $X_{IN}$ clock frequency | 1 | | 2.5 | MHz |
| $t_{XIN}$ | $X_{IN}$ clock period | 400 | | 1000 | ns |
| $t_1$ | $X_{IN}$ clock high | 0.4 × $t_{XIN}$ | | | ns |
| $t_2$ | $X_{IN}$ clock low | 0.4 × $t_{XIN}$ | | | ns |

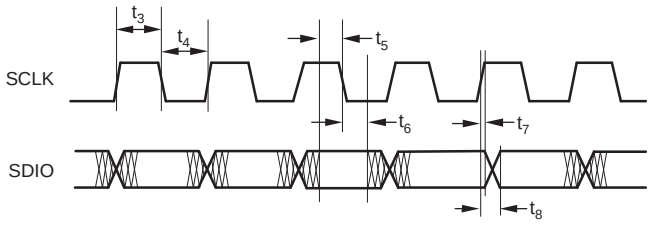



**Figure 8. Serial Input/Output Timing**

**Table 3. Serial I/O Timing Characteristics**

| SYMBOL | DESCRIPTION | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| $t_3$ | SCLK high | 5 × $t_{XIN}$ | | | ns |
| $t_4$ | SCLK low | 5 × $t_{XIN}$ | | | ns |
| $t_5$ | Data in valid to SCLK falling edge (setup) | 40 | | | ns |
| $t_6$ | SCLK falling edge to data in not valid (hold) | 20 | | | ns |
| $t_7$ | Data out valid to rising edge of SCLK (hold) | 0 | | | ns |
| $t_8$ | SCLK rising edge to new data out valid (delay) | | | 50 | ns |

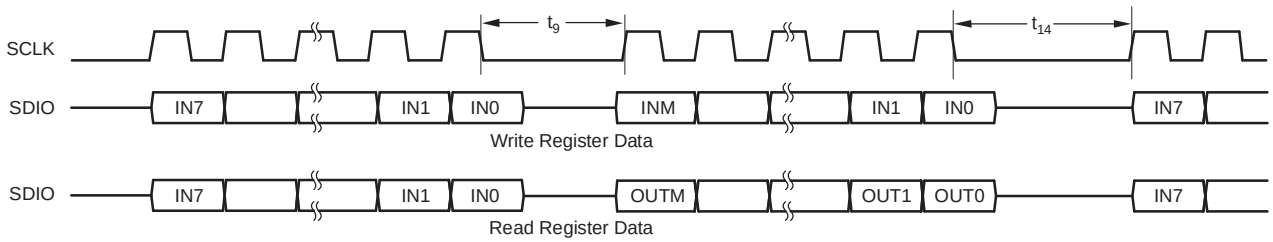



**Figure 9. Serial Interface Timing ($\overline{CS}$ Low)**

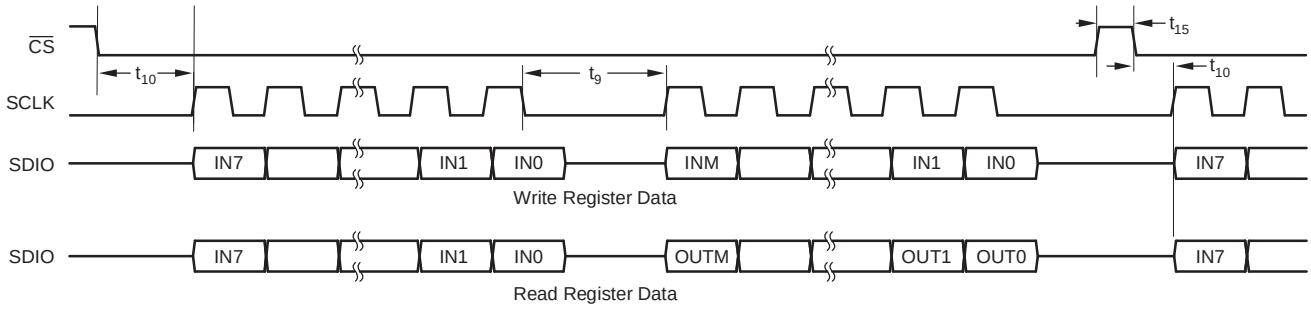



**Figure 10. Serial Interface Timing (Using $\overline{CS}$)**

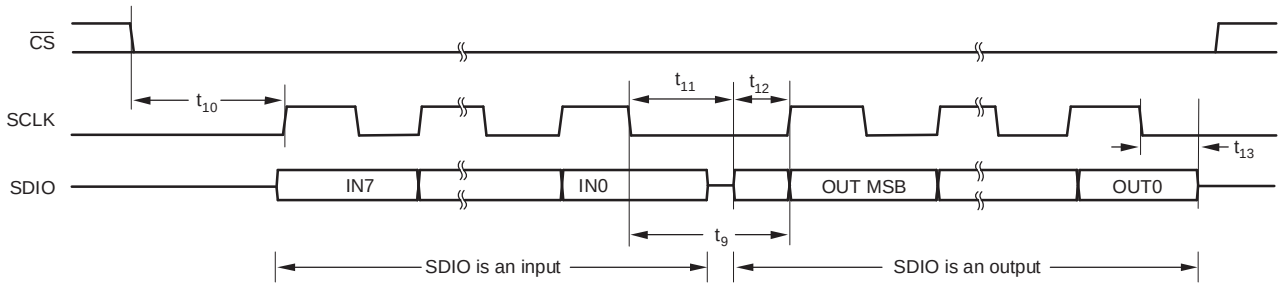



**Figure 11. SDIO Input to Output Transition Timing**

**Table 4. Serial Interface Timing Characteristics**

| SYMBOL | DESCRIPTION | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| $t_9$ | Falling edge of last SCLK for command to rising edge of first SCLK for register data | 13 × $t_{XIN}$ | | | ns |
| $t_{10}$ | Falling edge of $\overline{CS}$ to rising edge of SCLK | 11 × $t_{XIN}$ | | | ns |
| $t_{11}$ | Falling edge of last SCLK for command to SDIO as output | 8 × $t_{XIN}$ | | 10 × $t_{XIN}$ | ns |
| $t_{12}$ | SDIO as output to rising edge of first SCLK for register data | | 4 × $t_{XIN}$ | | ns |
| $t_{13}$ | Falling edge of last SCLK for register data to SDIO tri-state | 4 × $t_{XIN}$ | | 6 × $t_{XIN}$ | ns |
| $t_{14}$ | Falling edge of last SCLK for register data to rising edge of first SCLK of next command ($\overline{CS}$ tied low) | 41 × $t_{XIN}$ | | | ns |
| $t_{15}$ | Rising edge of $\overline{CS}$ to falling edge of $\overline{CS}$ (using $\overline{CS}$) | 22 × $t_{XIN}$ | | | ns |

The chip-select pin $\overline{CS}$ is active low. When $\overline{CS}$ is high, activity on SCLK is ignored. There are certain timing limits and delays which apply to the manipulation of $\overline{CS}$, as shown in Figure 10. These must be observed, or the DAC1220 may malfunction.

If $\overline{CS}$ is not used, it should be tied low. When $\overline{CS}$ is tied low, different timing limits and delays must be observed, as shown in Figure 9. If these are violated, the DAC1220 may malfunction.

The serial interface is byte-oriented. All data is transferred in groups of eight bits.

## I/O Recovery

The DAC1220 has a timeout on the serial interface. If $f_{CLK}$ is 2.5MHz, the timeout is approximately 100ms. At 2.5MHz, if a command is interrupted, and no activity occurs on the SCLK or $\overline{CS}$ lines for 100ms, the DAC1220 will cancel the command. If the command was a write command, no registers are affected.

The timeout period scales with the frequency of $f_{CLK}$.

## SCLK Reset Pattern

The DAC1220 does not have a dedicated reset pin. Instead, it contains a circuit which waits for a special pattern to appear on SCLK, and triggers the internal hardware reset line when it detects the special pattern.

This pattern, called the SCLK reset pattern, is shown in Figure 12, with timing information given in Table 5. The pattern is very different from the usual clocking patterns which appear on SCLK, and is unlikely to be detected by accident during normal operation.

The SCLK reset pattern can only be triggered when $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK line is ignored, and the SCLK reset pattern is not detected.

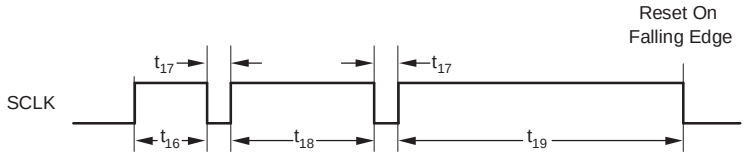



**Figure 12. Resetting the DAC1220**

**Table 5. Reset Timing Characteristics**

| SYMBOL | DESCRIPTION | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{16}$ | First high period | 512 × $t_{XIN}$ | | 800 × $t_{XIN}$ | ns |
| $t_{17}$ | Low period | 10 × $t_{XIN}$ | | | ns |
| $t_{18}$ | Second high period | 1024 × $t_{XIN}$ | | 1800 × $t_{XIN}$ | ns |
| $t_{19}$ | Third high period | 2048 × $t_{XIN}$ | | 2400 × $t_{XIN}$ | ns |

# PROGRAMMING

## Commands

Communication with the DAC1220 consists entirely of commands, which access the DAC1220 registers. Commands consist of a command byte followed by one, two or three data bytes. The data bytes can be sent to the DAC1220 or read from the DAC1220, depending on whether the command is a read command or a write command.

The format of the command byte is shown in Table 6, and the bits are described in Table 7. DAC1220 commands access the register map, which is shown in Table 11. A DAC1220 command can read or write one byte, or two or three adjacent bytes, in the register map.

## Bit and Byte Order

The order of the bits of data bytes in a command is configurable. The DAC1220 can be programmed to output data bytes MSB first or LSB first. The command byte is always transmitted MSB first. See the description of the MSB bit in Table 6 for further details. The order of the data bytes themselves is also configurable. See the description of the BD bit in Table 13 for details. Note that the BD bit does not affect the command byte; this always comes first.

## Registers

There are four registers in the DAC1220, as shown in the register map in Table 11. The Data Input Register (DIR) and the two calibration registers are 24 bits in length, and the Command Register (CMR), which contains configuration bits, is 16 bits in length.

## Modes

The DAC1220 has three operating modes: Sleep, Normal, and Self Calibration.

In Sleep mode, the DAC1220 output is off (high impedance), and much of the internal circuitry is switched off. In this mode the DAC1220 draws little power. The oscillator continues to run, however. Sleep is the mode entered after reset.

In Normal mode, the DAC1220 is fully active, and the output is on.

In Self Calibration mode, the DAC1220 runs its self-calibration sequence. After the sequence is complete, the DAC1220 switches to Normal mode. See the *Calibration* section for more information.

**Table 6. Command Byte Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | MB | | 0 | ADR | | | |

**Table 7. Command Byte Bits**

| BIT(S) | NAME | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | R/$\overline{W}$ | 0 | Write to register map |
| | | 1 | Read from register map |
| 6–5 | MB | | Number of bytes to read or write |
| | | 00b | 1 byte |
| | | 01b | 2 bytes |
| | | 10b | 3 bytes |
| | | 11b | Reserved; do not use |
| 3–0 | ADR | 0–15 | Start address in register map |

## Startup Sequence

At startup, the following procedure should generally be followed to properly initialize the DAC1220:

1. If the DAC1220 is being clocked from a crystal, wait for the oscillator to start—at least 25ms—before attempting to communicate with it. Trying to communicate with the DAC1220 before the crystal oscillator has reached its final frequency will usually result in corrupt communication.
2. Optionally apply the SCLK reset pattern. This should also only be done once the oscillator is started, since the pattern is detected using oscillator cycles. Applying the reset pattern at power-up ensures that the DAC1220 is reset properly, and not lingering in an unknown state in case of POR failure, brownout, etc. After a successful reset, the DAC1220 enters Normal mode.
3. Set up the Command Register as desired. This may include changing the mode from Sleep to Self Calibration or Normal.
4. Calibrate the DAC1220. Although this step is optional, the DAC1220 should almost always be calibrated. It is permissible to run calibration every time, or to use values from a previous calibration. See the *Calibration* section for details.

After calibration, the DAC1220 returns to Normal mode. The DAC1220 is ready to accept data once it is in Normal mode, but calibration or the use of saved calibration values is highly recommended.

## Calibration

Calibration is governed by two registers. The Offset Calibration Register (OCR) stores a value determining the offset calibration, and the Full-Scale Calibration Register (FCR) stores a value determining the gain calibration.

The value in the OCR is scaled and additive. It has a linear relationship to the generated offset calibration voltage. The value in the FCR is scaled and multiplicative. It has a linear relationship to the generated gain calibration multiplier.

Since the calibration functions are linear, calibration results can be averaged for greater precision. For example, it may be beneficial to perform several self-calibrations in succession, record the result of each, average them together, and store the averages in the OCR and FCR.

## Self-Calibration Procedure

To perform a self-calibration, place the DAC1220 into Self Calibration mode by setting the MD1 bit to '0' and the MD0 bit to '1' in the Command Register. At a clock frequency of 2.5MHz, self-calibration takes between 300ms and 500ms; the actual time is indeterminate and depends on the results.

If the CALPIN bit in the Command Register is '1', the output remains connected during calibration. The DAC voltage will change during the calibration process. This can be important if the DAC output is loaded significantly; disconnecting the output during calibration places a high load impedance on the output amplifier, which may be different from normal operation.

If the CALPIN bit in the Command Register is '0', the output will be disconnected during calibration. If this is the case, when calibration begins, the DAC1220 briefly charges the $C_2$ capacitor to the current output voltage. If the output is buffered, $C_2$ effectively becomes a sample-and-hold capacitor, so that the final output voltage remains during calibration.

When the calibration is complete, the DAC1220 switches to Normal mode. If the output was disconnected, it is reconnected at that time. The end of the calibration procedure can be detected by polling the MD1 and MD0 bits. When they become 0, the calibration is complete.

If readback is not being performed, simply wait at least 500ms before sending further commands to the device, assuming that the clock frequency is 2.5MHz.

Once calibration is complete, the OCR and FCR contain the results of the calibration, and the new constants are effective immediately.

## Setting the Output Voltage

To set the DAC1220 output voltage, write a code to the Data Input Register (DIR). A write to any of the bytes in the DIR causes the voltage to change at the completion of the write command.

The DAC1220 operates in either 16- or 20-bit mode. The DIR is 24 bits wide, and the code stored in it is left justified, with the least significant bits ignored. Therefore, in 16-bit mode, only the upper 16 bits of the DIR are significant, and in 20-bit mode, only the upper 20 bits of the DIR are significant.

In 20-bit mode, all three bytes of the DIR must be written to in order to completely update the code. In 16-bit mode, it is only necessary to write to the two upper bytes; a write to the lower byte has no effect on the output.

The code may be given in either straight binary or offset two's complement format. This is controlled by the DF bit in the Command Register (see the register description in Table 13 for details). The two data format options and the 16- or 20-bit option give rise to four transfer functions, which are shown in Table 8. For reference, several ideal output voltages for given input codes are shown in Table 9.

Note that the DIR code can also be considered a 24-bit number. This may be convenient in software. In this case the transfer functions for 16- and 20-bit modes are the same, except that in 16-bit mode the code is truncated by eight bits, and in 20-bit mode the code is truncated by four bits.

**Table 8. Transfer Functions**

| DATA FORMAT | 20-BIT MODE | 16-BIT MODE |
|---|---|---|
| Offset two's complement | $V_{OUT} = 2V_{REF}\frac{code + 2^{19}}{2^{20}}$ | $V_{OUT} = 2V_{REF}\frac{code + 2^{15}}{2^{16}}$ |
| Straight binary | $V_{OUT} = 2V_{REF}\frac{code}{2^{20}}$ | $V_{OUT} = 2V_{REF}\frac{code}{2^{16}}$ |

**Table 9. Example Output Voltages**

| APPROXIMATE OUTPUT VOLTAGE | RESOLUTION | DATA FORMAT | CODE | DIR CONTENT (1) |
|---|---|---|---|---|
| 0V | 16-bit | Two's complement | 8000h | 8000xxh |
| | | Straight binary | 0000h | 0000xxh |
| | 20-bit | Two's complement | 8000h | 80000xh |
| | | Straight binary | 0000h | 00000xh |
| 2.5V | 16-bit | Two's complement | 0000h | 0000xxh |
| | | Straight binary | 8000h | 8000xxh |
| | 20-bit | Two's complement | 0000h | 00000xh |
| | | Straight binary | 8000h | 80000xh |
| 5V | 16-bit | Two's complement | 7FFFh | 7FFFxxh |
| | | Straight binary | FFFFh | FFFFxxh |
| | 20-bit | Two's complement | 7FFFFh | 7FFFFxh |
| | | Straight binary | FFFFFh | FFFFFxh |

(1) x = Do not care

## Fast Settling Mode

To speed up settling, the DAC1220 can change the cutoff frequency of its output filter. Raising the cutoff frequency causes the DAC1220 to settle faster, but at the expense of higher noise. The adaptive filtering mode provides a good compromise by increasing the filter frequency only while the DAC is changing its output by more than approximately 40mV. When the output has settled, the filter frequency is reduced again.

Adaptive filtering is controlled by the ADPT and DISF bits in the Command Register. The action of these bits together is described in Table 10.

**Table 10. Fast Settling Modes**

| ADPT (CMR bit 15) | DISF (CMR bit 4) | FAST SETTLING MODE |
|---|---|---|
| 0 | 0 | Fast settling only during > 40mV step |
| 0 | 1 | Disabled |
| 1 | 0 | Fast settling always on (filter cutoff increased) |
| 1 | 1 | Disabled |

## REGISTERS

The register map is shown in Table 11.

**Table 11. Register Memory Map**

| ADDRESS | CONTENT |
|---|---|
| 0 | DIR byte 2 (MSB) |
| 1 | DIR byte 1 |
| 2 | DIR byte 0 (LSB) |
| 3 | Reserved |
| 4 | CMR byte 1 (MSB) |
| 5 | CMR byte 0 (LSB) |
| 6 | Reserved |
| 7 | Reserved |
| 8 | OCR byte 2 (MSB) |
| 9 | OCR byte 1 |
| 10 | OCR byte 0 (LSB) |
| 11 | Reserved |
| 12 | FCR byte 2 (MSB) |
| 13 | FCR byte 1 |
| 14 | FCR byte 0 (LSB) |
| 15 | Reserved |

### Command Register (CMR)

The command register contains the configuration bits of the DAC1220. It is shown in Table 12. The bits in the command register are shown in Table 13.

Writes to the CMR take effect at the negative edge of SCLK during the last bit of the last byte of the write command.

**Table 12. Command Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADPT | CALPIN | Reserved | Reserved | Reserved | Reserved | CRST | Reserved |
| R/W-0 | R/W-0 | R-1(1) | R-0 | R-1 | R-0 | R/W-0 | R-0 |

(1) In early versions of the DAC1220, this bit was rw-0. See the *Calibration* section for details.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RES | CLR | DF | DISF | BD | MSB | MD | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-10b | |

LEGEND: R = Read, W = Write

**Table 13. Command Register Bits**

| BIT(S) | NAME | VALUE | DESCRIPTION |
|---|---|---|---|
| 15 | ADPT | | Controls adaptive filtering. if DISF is set, this bit has no effect. |
| | | 0 | Adaptive filtering enabled (default). |
| | | 1 | Adaptive filtering disabled. |
| 14 | CALPIN | 0 | Output is disconnected (high impedance) during calibration (default). |
| | | 1 | Output is connected during calibration. |
| 13 | Reserved | | Write '1' to this bit. On early versions of the device, this bit is writable and defaults to zero, but still should be set to '1'. On current devices this bit is read-only and always reads '1'. See the *Calibration* section for details. |
| 12 | Reserved | | Read-only. Always '0'. |
| 11 | Reserved | | Read-only. Always '0'. |
| 10 | Reserved | | Read-only. Always '0'. |
| 9 | CRST | | In Normal mode, writing '1' to this bit resets the calibration registers, setting OCR to 000000h and FCR to 800000h. In Normal mode, this bit always reads '0'.<br>In Sleep mode, this bit is read/write, and has no effect.<br>Writing '1' to this bit and switching to Normal mode at the same time will reset the calibration registers. |
| | | 0 | Do not clear calibration registers. |
| | | 1 | Clear calibration registers. |
| 8 | Reserved | | Read-only. Always '0'. |
| 7 | RES | | Selects resolution. |
| | | 0 | 16-bit resolution (default). |
| | | 1 | 20-bit resolution. |
| 6 | CLR | | In Normal mode, writing '1' to this bit writes 0 to the data register.<br>In Sleep mode, this bit is read/write, and has no effect.<br>Writing '1' to this bit and switching to Normal mode at the same time will reset the data register.<br>The actual voltage that the DAC1220 will output on setting this bit depends on the data format selected by DF. If DF is 1, zero gives 0V; if DF is 0, zero gives $V_{REF}$ (mid-scale). |
| | | 0 | Do not clear calibration registers. |
| | | 1 | Clear calibration registers. |
| 5 | DF | | Selects binary number format of the data register. |
| | | 0 | Offset two's complement (default). |
| | | 1 | Straight binary. |
| 4 | DISF | | Can be used to inhibit fast settling and/or adaptive filtering. See text for details. |
| | | 0 | Fast settling and/or adaptive filtering enabled (default). |
| | | 1 | Fast settling disabled; filter always at default cutoff. |
| 3 | BD | | Selects address increment or decrement when reading or writing multiple bytes, except when writing to the command register. The command register is always written to in increment mode (most significant byte first). Reads from the command register are according to this bit. |
| | | 0 | Address is incremented after each byte (default). |
| | | 1 | Address is decremented after each byte. |

**Table 13. Command Register Bits (continued)**

| BIT(S) | NAME | VALUE | DESCRIPTION |
|---|---|---|---|
| 2 | MSB | | Selects the order in which bits are shifted in and out of the DAC1220, except when writing to the command register. The command register is always written to MSB first. Reads from the command register are according to this bit. |
| | | 0 | Data is shifted MSB first (default). |
| | | 1 | Data is shifted LSB first. |
| 1-0 | MD | | Operating mode. |
| | | 00b | Normal mode (default). |
| | | 01b | Self calibration mode. (No other bits should be changed in the Command Register when setting this mode.) |
| | | 10b | Sleep mode. |
| | | 11b | Reserved. |

### Data Input Register (DIR)

The Data Input Register determines the output voltage in Normal mode.

In Sleep mode, writing to this register has no effect on the output, but the value is stored. The value in the DIR becomes effective immediately upon entering Normal mode.

After reset, the DIR contains zero.

See the section, *Setting the Output Voltage* for further details about the Data Input Register.

### Offset Calibration Register (OCR)

The Offset Calibration Register contains a 24-bit two's complement value. This value is added to the value in the DIR before conversion by the DAC.

In Sleep mode, writing to this register has no effect on the output, but the value is stored. The value in the OCR becomes effective immediately upon entering Normal mode.

After reset, the OCR contains zero. See the *Calibration* section for further details about the OCR.

### Full-Scale Calibration Register (FCR)

The Full-Scale Calibration Register stores the gain calibration constant. The content of the DIR is adjusted multiplicatively by this value before conversion by the DAC.

In Sleep mode, writing to this register has no effect on the output, but the value is stored. The value in the FCR becomes effective immediately upon entering Normal mode.

After reset, the FCR contains 800000h.

See the *Calibration* section for further details about the FCR.

## APPLICATION INFORMATION

### Layout Recommendations

The DAC1220 is a high-precision analog component incorporating digital elements. Achieving good precision is not difficult, but achieving excellent precision may require several attempts.

It is critical to supply a guard ring, or fill, around the $C_1$ and $C_2$ pins. The guard ring should be connected to the voltage reference. These nodes are very sensitive, and are good places for noise to couple through to the output. A ground fill on the opposite side of the board, or a ground plane, is also a good idea.

The capacitors themselves should be placed as near the pins as possible. In particular, the traces leading from $C_1$ and $C_2$ should be kept very short. The traces leading to $V_{OUT}$ and $V_{REF}$ can be longer.

It is also very important to route digital traces away from analog traces, so that their associated return currents will not couple into the analog side.

If a crystal is used, do not route the traces connecting the crystal to the device through vias, if possible, because this will increase the trace inductance and may affect startup and reliability. Keep the traces short, and place the crystal close to the device. Keep in mind that extra ground planes and trace lengths increase parasitic capacitance, and this should be deducted from the load capacitor values.

### Software Considerations

A key to communicating successfully with the DAC1220 is observing the delays in the interface timing diagrams. A violation of these delays, at best, results in lack of correct output; at worse, violating the delays can corrupt communications entirely.

Note that the delays are slightly different if chip-select ($\overline{CS}$) is not being used.

Timing delays from the beginning of an SPI byte transmission are a common problem in microcontroller firmware that uses an SPI peripheral. Be sure that any delay routine begins once a byte has completed transmission, or add the byte transmission time to the delay time.

Some programmers may find that *bit-banging*, or direct manipulation of microcontroller I/O pins, is the easiest way to communicate with the DAC1220, because of the delays and direction changes required.

### Write-Only Interfacing

In some situations, such as isolated interfacing, it is inconvenient to use the DAC1220 bidirectionally, since the SDIO pin changes direction for readback. The DAC1220 can be used write-only. The following considerations apply:

- When used write-only, it is not possible to verify that the DAC1220 is operating using its serial interface alone. The operation of the DAC is open-loop.
- It may be helpful to wait at least 150ms-200ms after startup. This ensures that, in case the reset was a result of firmware problems and not power-up, any previous communication with the DAC has been cancelled by the I/O recovery timeout.
- When applying the SCLK reset pattern, which can be done in place of the above steps, allow time for the oscillator to start before applying the pattern. The pattern is detected based on oscillator cycles, so it will not be detected if the oscillator is not yet running.

## Isolation

The DAC1220 serial interface allows for connection using as few as two wires. This is an advantage when galvanic isolation is required. An example isolated connection is shown in Figure 13. Here, chip-select is unused and therefore grounded, and the DAC1220 is being operated unidirectionally.

## DAC1220 Revisions

As of this writing, there have been two released revisions of the DAC1220. The only difference between the two versions is bit 13 of the Command Register. In the first revision, this bit was writable, and defaulted to '0'. In the current revision, which was released in 1999, this bit is fixed at '1', and is not writable.

For first revision chips, always write a '1' to this bit. Although the bit is not critical, performance is not optimal unless this bit is set.

This does no harm in current revision chips, and ensures that first revision chips perform optimally.

## Definition of Terms

**Differential Nonlinearity Error**—The difference between an actual step width and the ideal value of 1LSB. If the step width is exactly 1LSB, the differential nonlinearity error is zero. A differential nonlinearity specification of less than 1LSB ensures monotonicity.

**Drift**—The change in a parameter over temperature.

**Full-Scale Range (FSR)**—This is the magnitude of the typical analog output voltage range, which is 2 × $V_{REF}$. For example, when the converter is configured with a 2.5V reference, the Full-Scale range is 5.0V.

**Gain Error**—This error represents the difference in the slope between the actual and ideal transfer functions.

**Linearity Error**—The deviation of the actual transfer function from an ideal straight line between the data end points.

**Least Significant Bit (LSB) Weight**—This is the ideal change in voltage that the analog output changes with a change in the digital input code of 1LSB.

**Monotonicity**—Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes.

**Offset Error**—The difference between the expected and actual output, when the output is zero. The value is calculated from measurements made when $V_{OUT}$ = 20mV.

**Settling Time**—The time it takes the output to settle to a new value after the digital code has been changed.

**$f_{XIN}$** —The frequency of the crystal oscillator or CMOS-compatible input signal at the $X_{IN}$ input of the DAC1220.

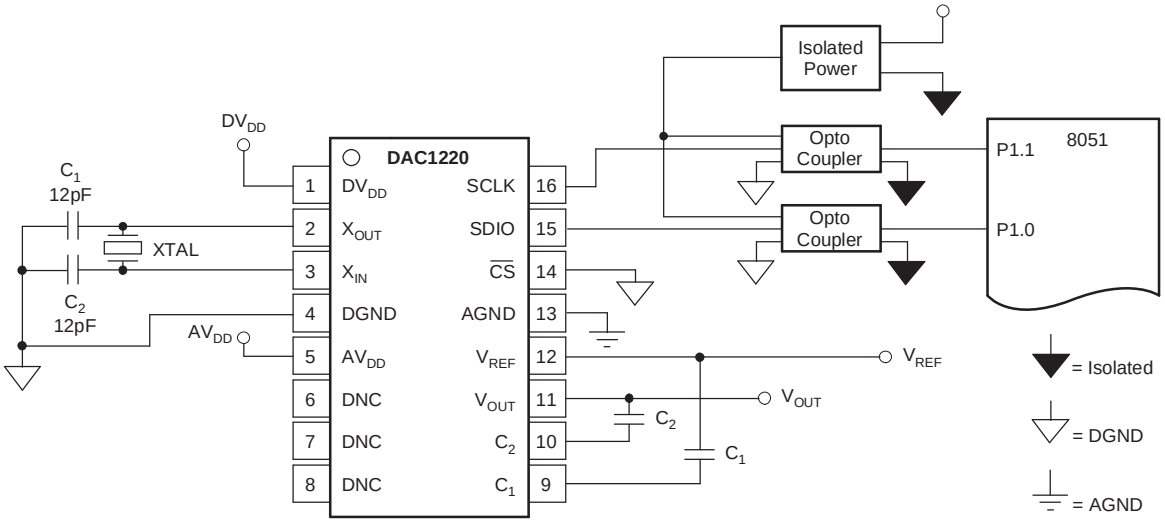



**Figure 13. Isolation for Two-Wire Interface**

## REVISION HISTORY

**Changes from Revision F (March, 2008) to Revision G** **Page**

- Revised Table 4, *Serial Interface Timing Characteristics*; changed *INSR* to *command* for all occurrences ..... 10

**Changes from Revision E (December 2007) to Revision F** **Page**

- Updated device graphic to TI logo ..... 1
- Changed description of the 01b row in the 1-0 bits section of Table 13 ..... 16

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC1220E | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DAC 1220E | Samples |
| DAC1220E/2K5 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DAC 1220E | Samples |
| DAC1220E/2K5G4 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DAC 1220E | Samples |
| DAC1220EG4 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DAC 1220E | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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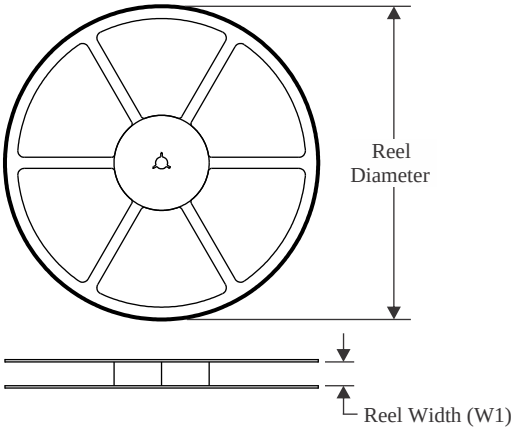
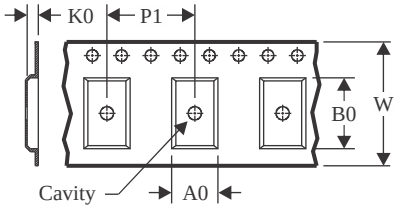
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

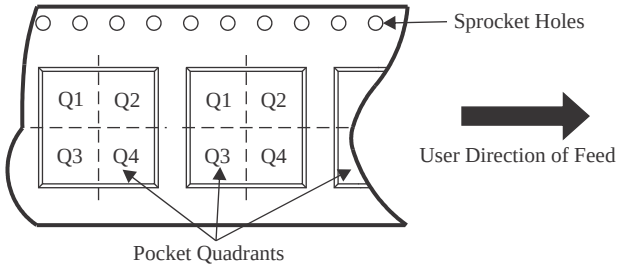



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

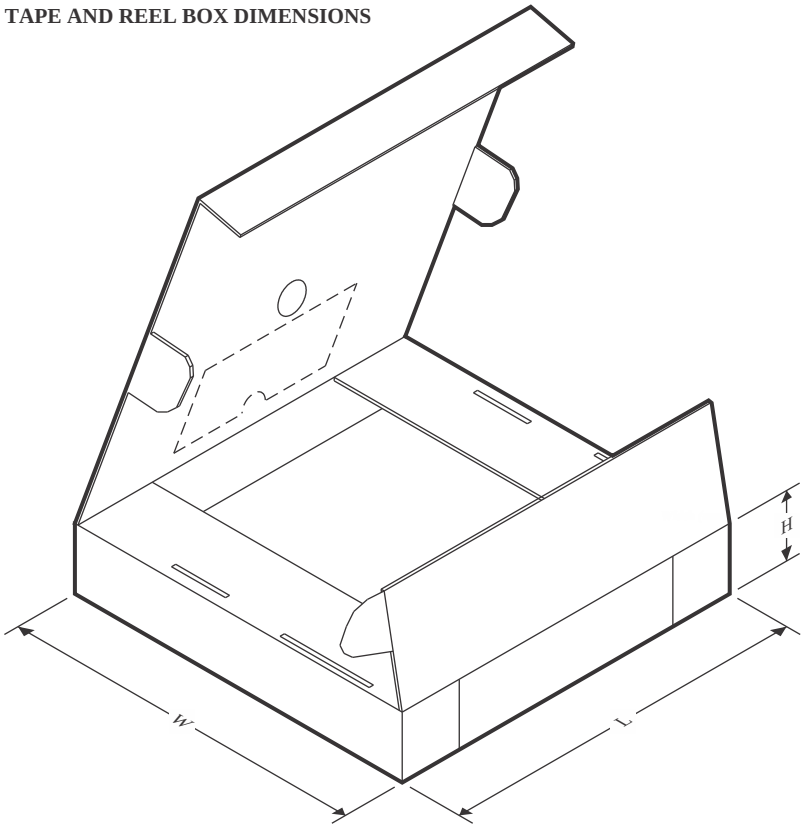
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC1220E/2K5 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

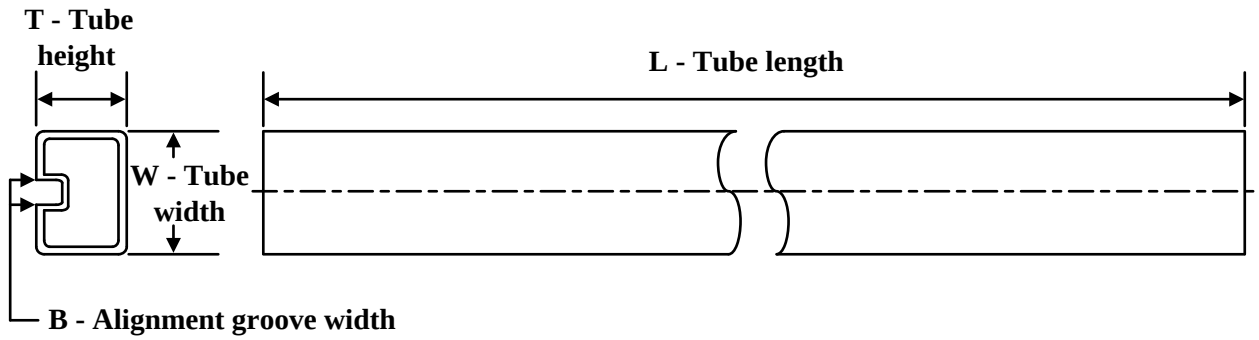
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

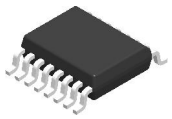
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DAC1220E/2K5 | SSOP | DBQ | 16 | 2500 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| DAC1220E | DBQ | SSOP | 16 | 75 | 506.6 | 8 | 3940 | 4.32 |
| DAC1220EG4 | DBQ | SSOP | 16 | 75 | 506.6 | 8 | 3940 | 4.32 |

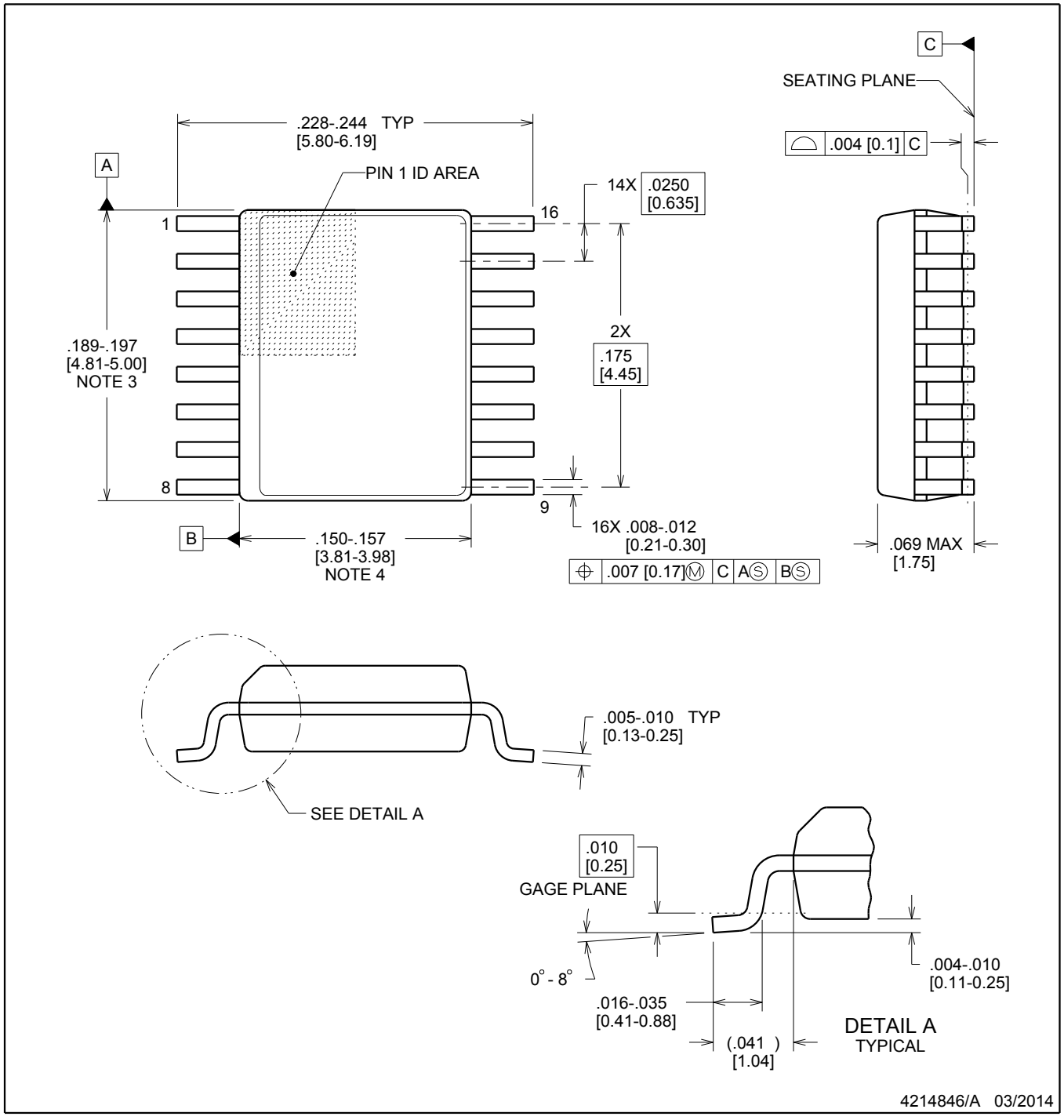


# PACKAGE OUTLINE

## DBQ0016A

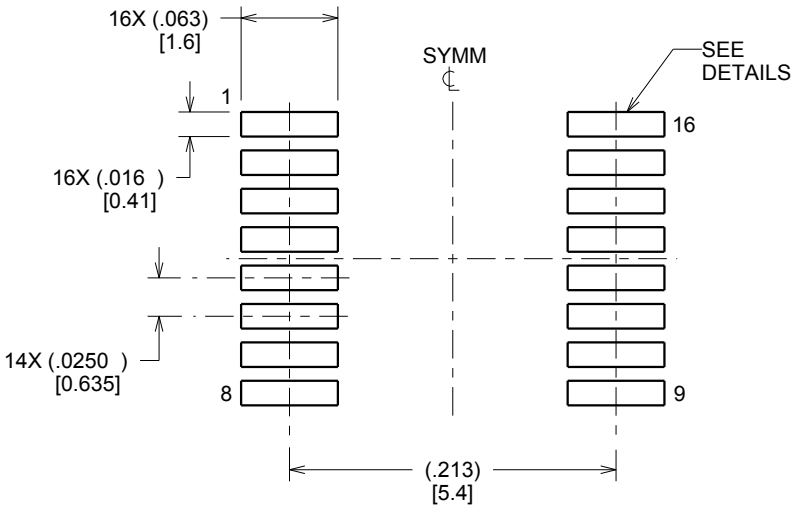
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

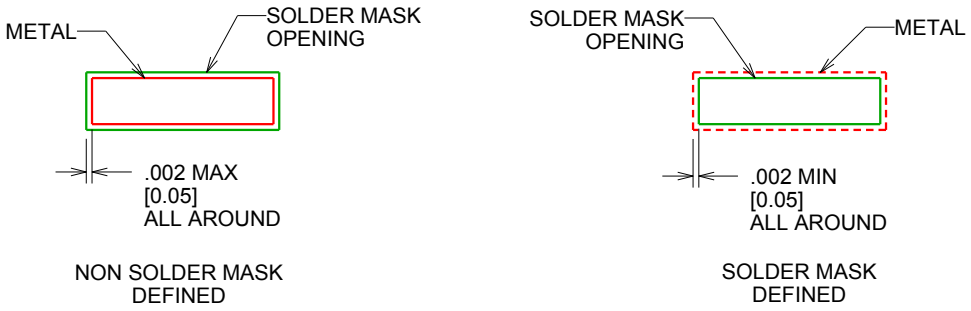



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

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NOTES: (continued)

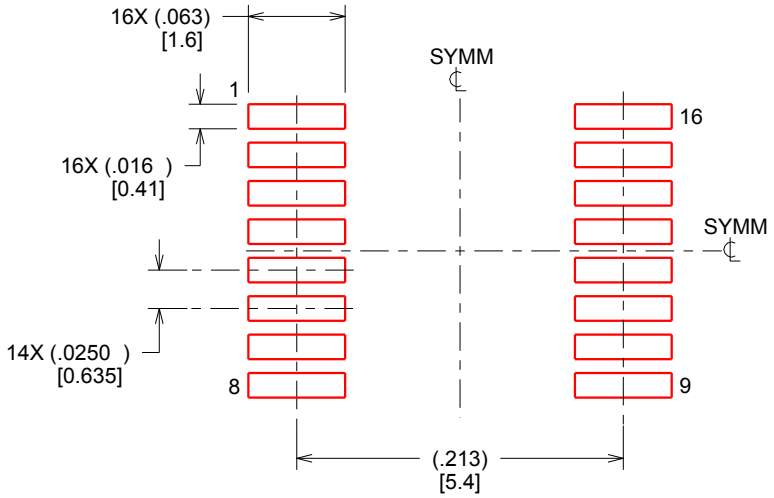
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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