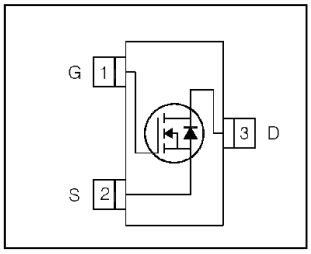
HEXFET® Power MOSFET

V_{DSS}	60	V
V_{GS}	±16	V
$R_{DS(on)}$ max (@ V_{GS} = 10V)	92	mΩ
$R_{DS(on)}$ max (@ V_{GS} = 4.5V)	116	mΩ



Micro 3™ (SOT-23)
IRLML0060TRPbF

G	D	S
Gate	Drain	Source

Applications

- Load/System Switch

Features		Benefits
Industry-Standard Pinout		Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques	results in	Easier Manufacturing
RoHS Compliant Containing no Lead, no Bromide and no Halogen	⇒	Environmentally Friendlier
MSL1		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLML0060TRPbF	Micro 3™ (SOT-23)	Tape and Reel	3000	IRLML0060TRPbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	60	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	2.7	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	2.1	
I_{DM}	Pulsed Drain Current	11	
P_D @T_A= 25°C	Maximum Power Dissipation	1.25	W
P_D @T_A= 70°C	Maximum Power Dissipation	0.80	
	Linear Derating Factor	0.01	mW/°C
V_{GS}	Gate-to-Source Voltage	± 16	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	100	°C/W
$R_{\theta JA}$	Junction-to-Ambient (t < 10s) ④	—	99	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	98	116	mΩ	V_{GS} = 4.5V, I_D = 2.2A
		—	78	92		V_{GS} = 10V, I_D = 2.7A
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 25µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 60V, V_{GS} = 0V
		—	—	250		V_{DS} = 60V,V_{GS} = 0V,T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
R_G	Internal Gate Resistance	—	1.6	—	Ω	
gfs	Forward Trans conductance	7.6	—	—	S	V_{DS} = 25V, I_D = 2.7A
Q_g	Total Gate Charge	—	2.5	—	nC	I_D = 2.7A
Q_{gs}	Gate-to-Source Charge	—	0.7	—		V_{DS} = 30V
Q_{gd}	Gate-to-Drain (‘Miller’) Charge	—	1.3	—		V_{GS} = 4.5V ②
$t_{d(on)}$	Turn-On Delay Time	—	5.4	—	ns	V_{DD} = 30V②
t_r	Rise Time	—	6.3	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	6.8	—		R_G = 6.8Ω
t_f	Fall Time	—	4.2	—		V_{GS} = 4.5V
C_{iss}	Input Capacitance	—	290	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	37	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	21	—		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	11		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 2.7A,V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	14	21	ns	T_J = 25°C ,V_R = 30V, I_F = 1.6A
Q_{rr}	Reverse Recovery Charge	—	13	20	nC	di/dt = 100A/µs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 400µs; duty cycle ≤ 2%.
③ Surface mounted on 1 in square Cu board
④ Refer to application note #AN-994.

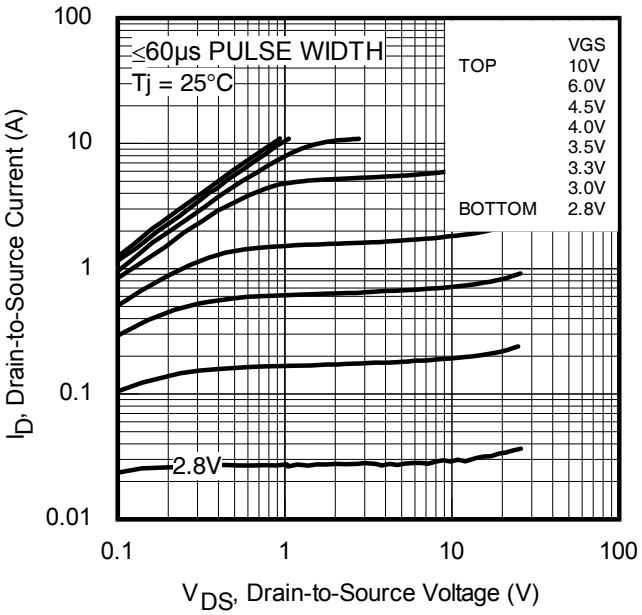


Fig. 1 Typical Output Characteristics

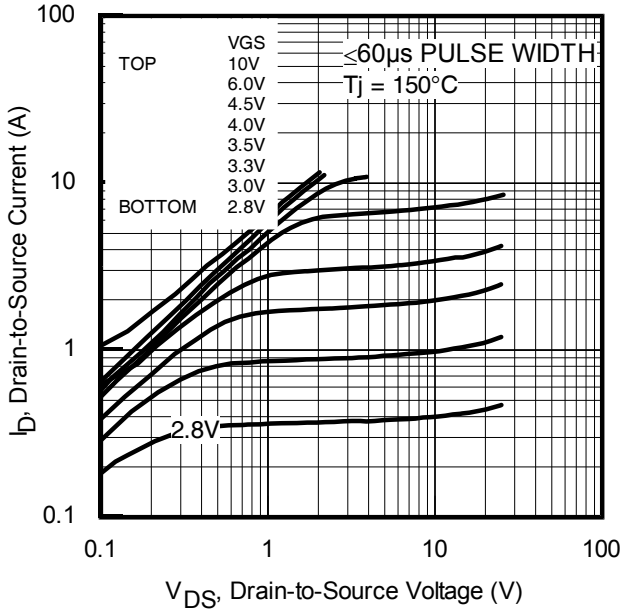


Fig. 2 Typical Output Characteristics

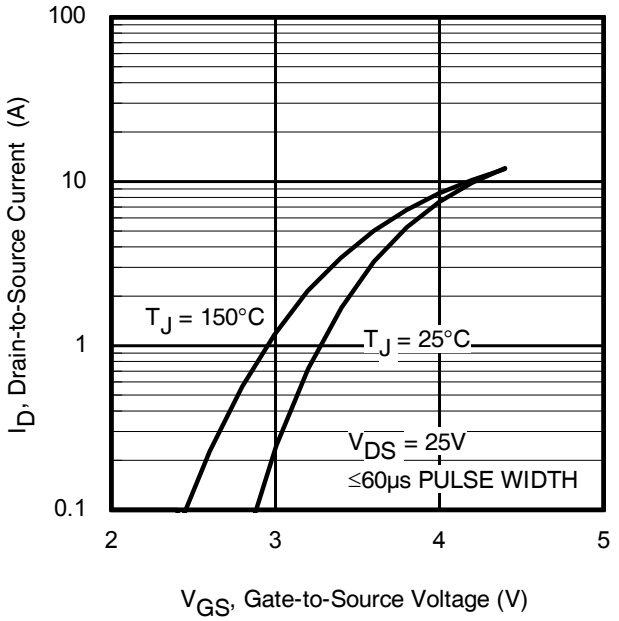


Fig. 3 Typical Transfer Characteristics

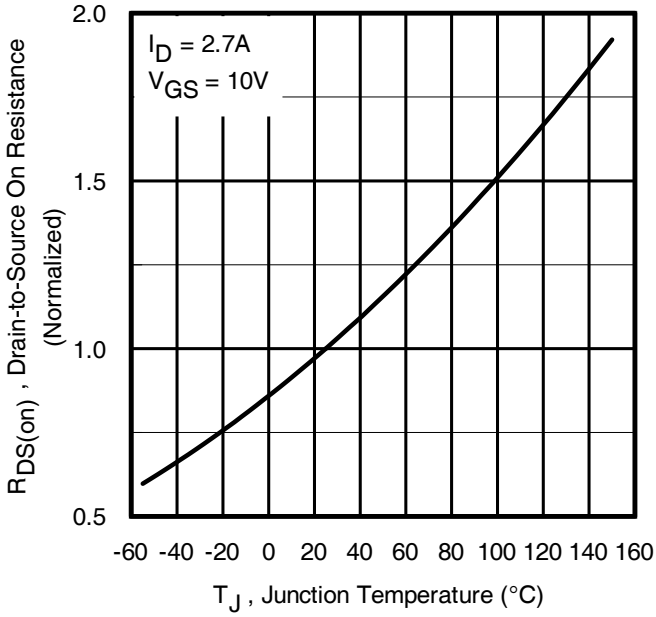


Fig. 4 Normalized On-Resistance vs. Temperature

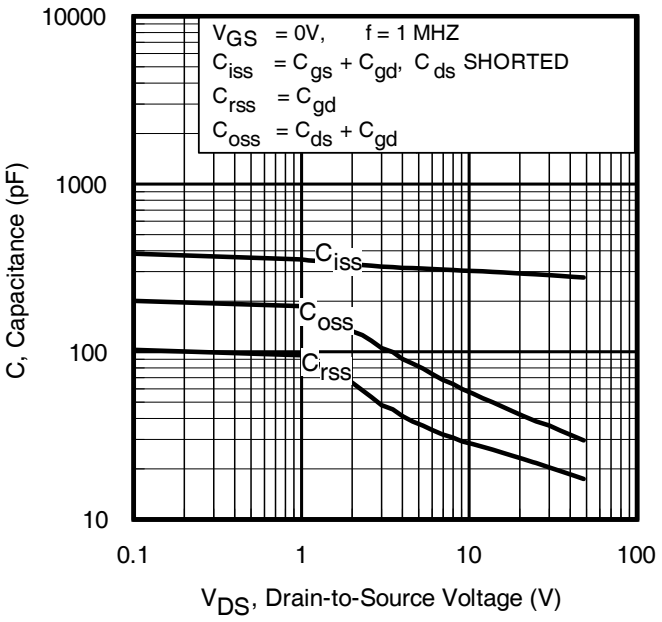


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

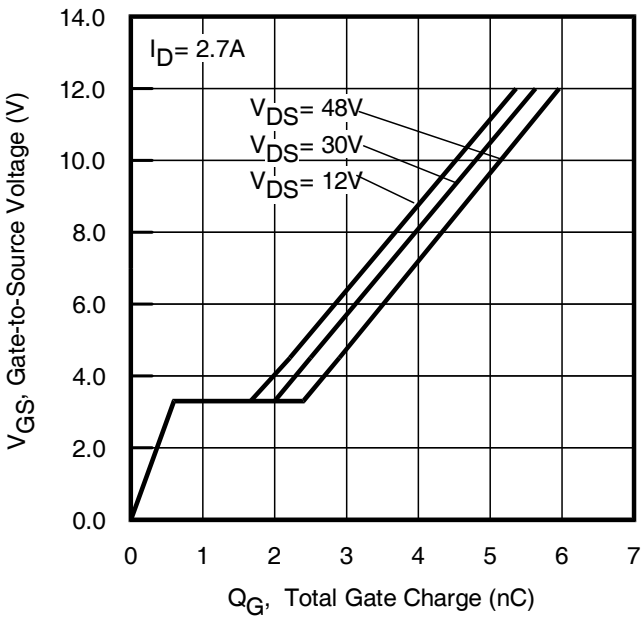


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

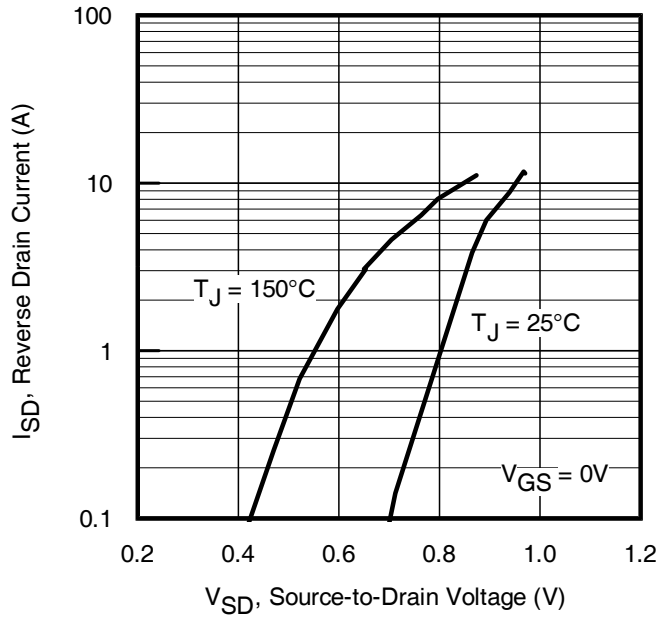


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

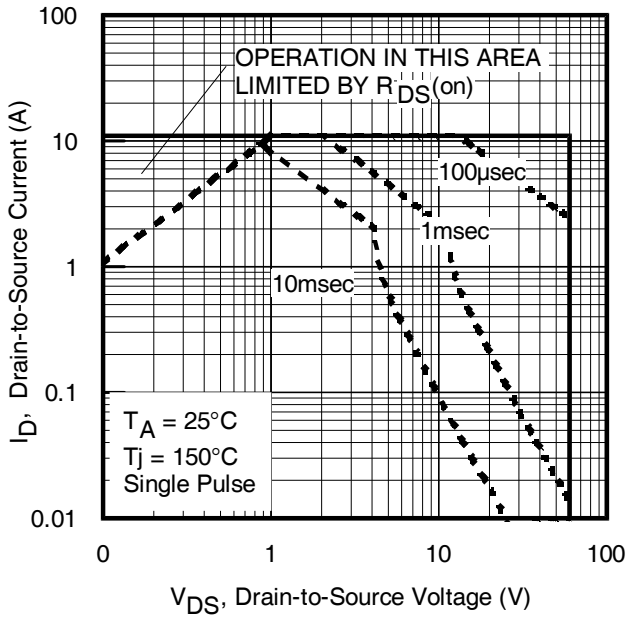


Fig 8. Maximum Safe Operating Area

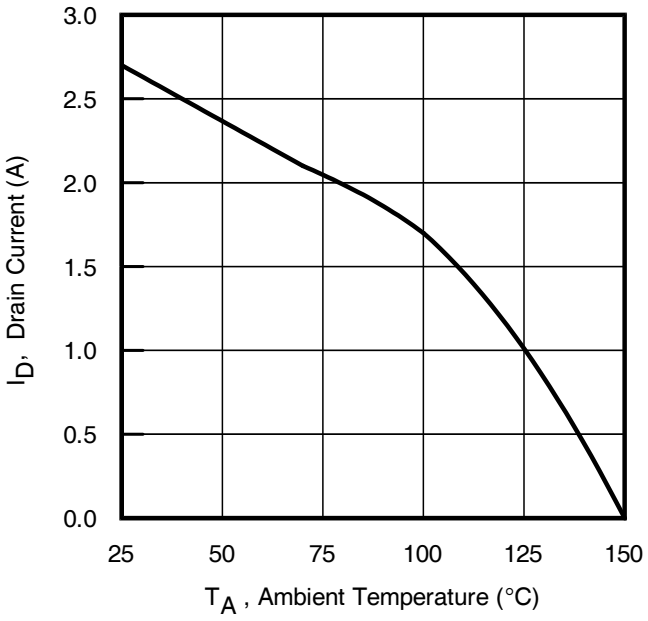


Fig 9. Maximum Drain Current vs. Case Temperature

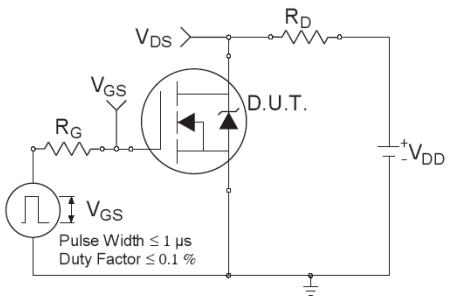


Fig 10a. Switching Time Test Circuit

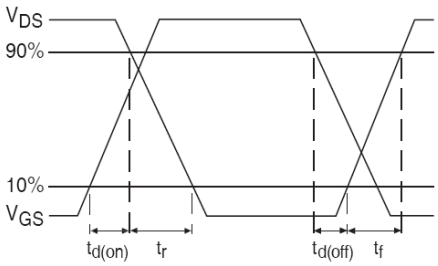


Fig 10b. Switching Time Waveforms

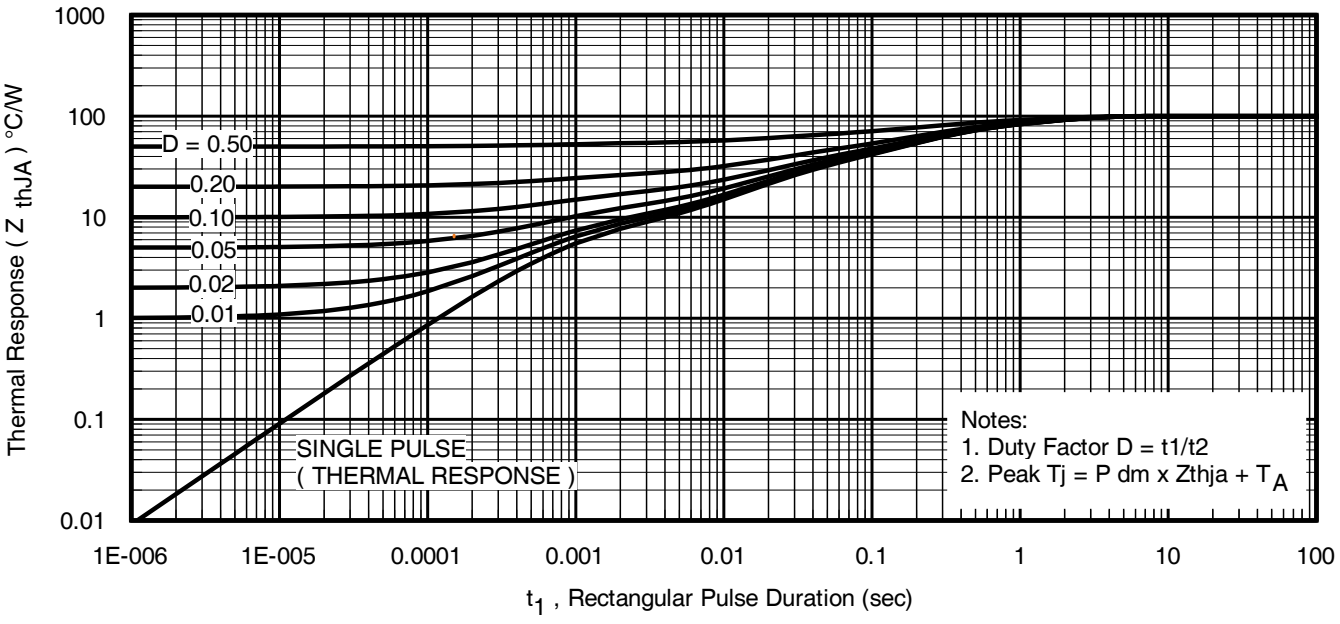


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

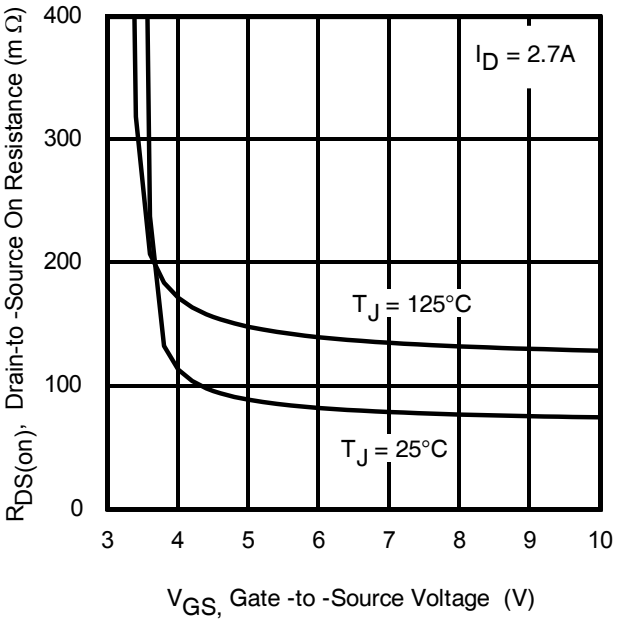


Fig 12. Typical On-Resistance Vs. Gate Voltage

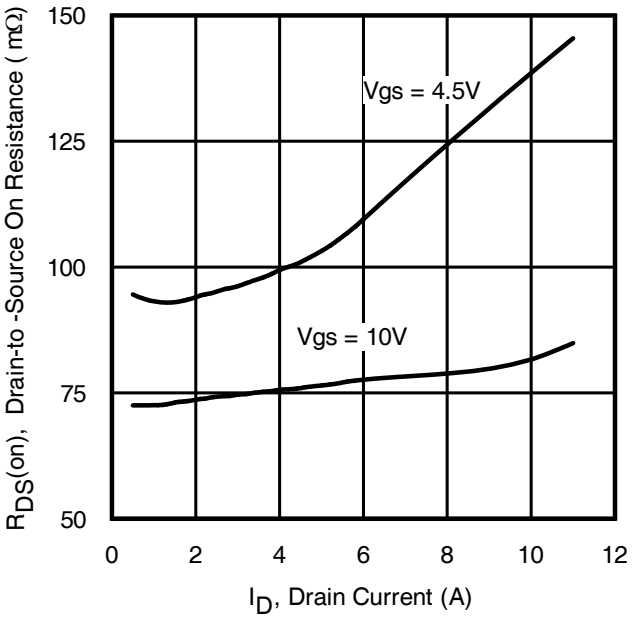


Fig 13. Typical On-Resistance Vs. Drain Current

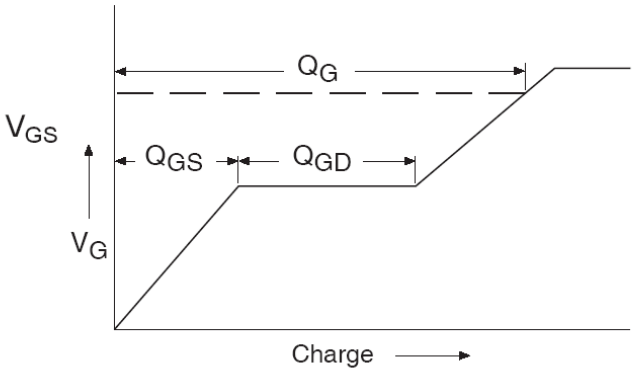


Fig 14a. Basic Gate Charge Waveform

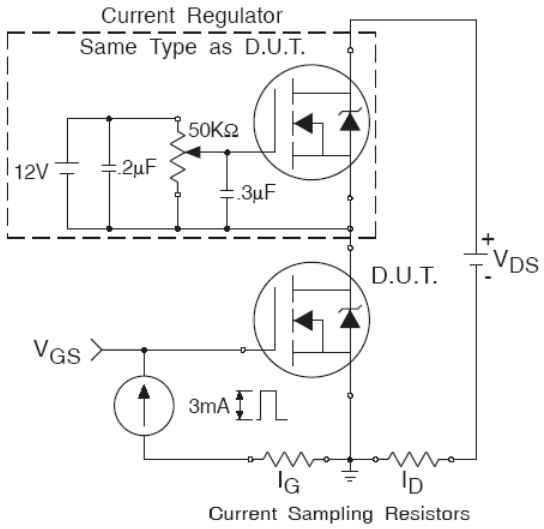


Fig 14b. Gate Charge Test Circuit

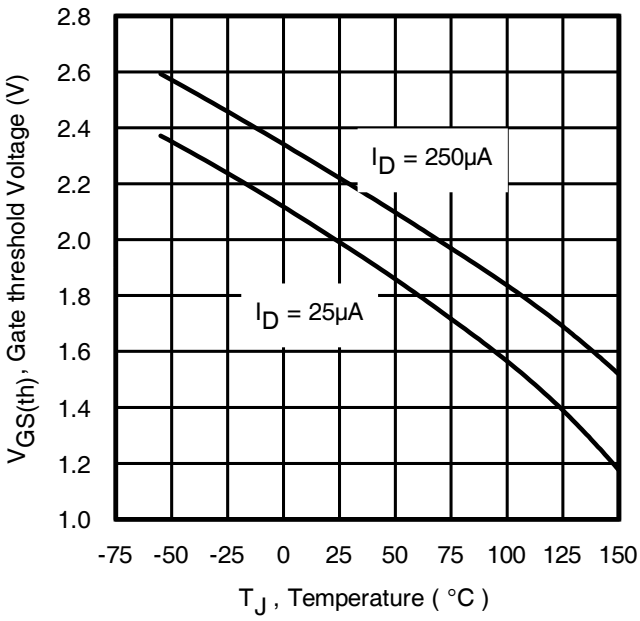


Fig 15. Typical Threshold Voltage Vs. Junction Temperature

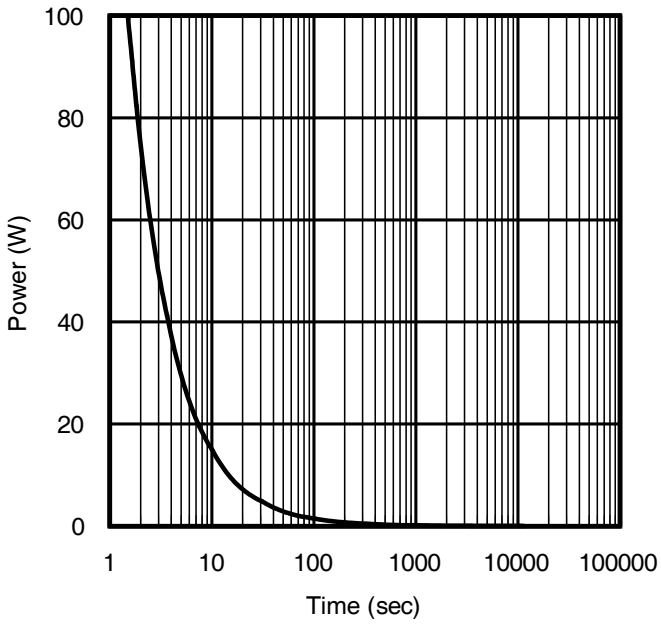
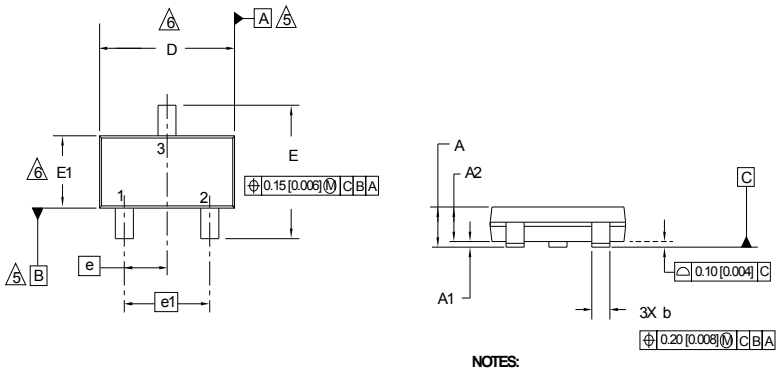
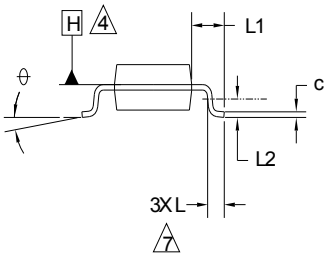


Fig 16. Typical Power Vs. Time

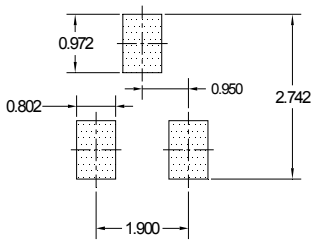
Micro3™ (SOT-23) Package Outline (Dimensions are shown in millimeters (inches))



DIMENSIONS				
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.89	1.12	0.035	0.044
A1	0.01	0.10	0.0004	0.004
A2	0.88	1.02	0.035	0.040
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E1	1.20	1.40	0.047	0.055
e	0.95	BSC	0.037	BSC
e1	1.90	BSC	0.075	BSC
L	0.40	0.60	0.016	0.024
L1	0.54	REF	0.021	REF
L2	0.25	BSC	0.010	BSC
θ	0	8	0	8



Recommended Footprint

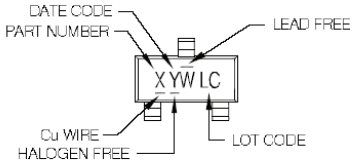


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE MOLD PARTING LINE.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H. DIMENSIONS DOES NOT INCLUDE MOLD PROTRUSIONS OR INTERLEAD FLASH. MOLD PROTRUSIONS OR INTERLEAD FLASH SHALL NOT EXCEED 0.25 MM [0.010 INCH] PER SIDE.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-236 AB.

Micro3™ (SOT-23/TO-236AB) Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001



X = PART NUMBER CODE REFERENCE:

A = IRLML2402	S = IRLML6244
B = IRLML2803	T = IRLML6246
C = IRLML6302	U = IRLML6344
D = IRLML5103	V = IRLML6346
E = IRLML6402	W = IRFML8244
F = IRLML6401	X = IRLML2244
G = IRLML2502	Y = IRLML2246
H = IRLML5203	Z = IRFML9244
I = IRLML0030	
J = IRLML2030	
K = IRLML0100	
L = IRLML0060	
M = IRLML0040	
N = IRLML2060	
P = IRLML9301	
R = IRLML9303	

Note: A line above the work week (as shown here) indicates Lead - Free.

DATE CODE MARKING INSTRUCTIONS

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

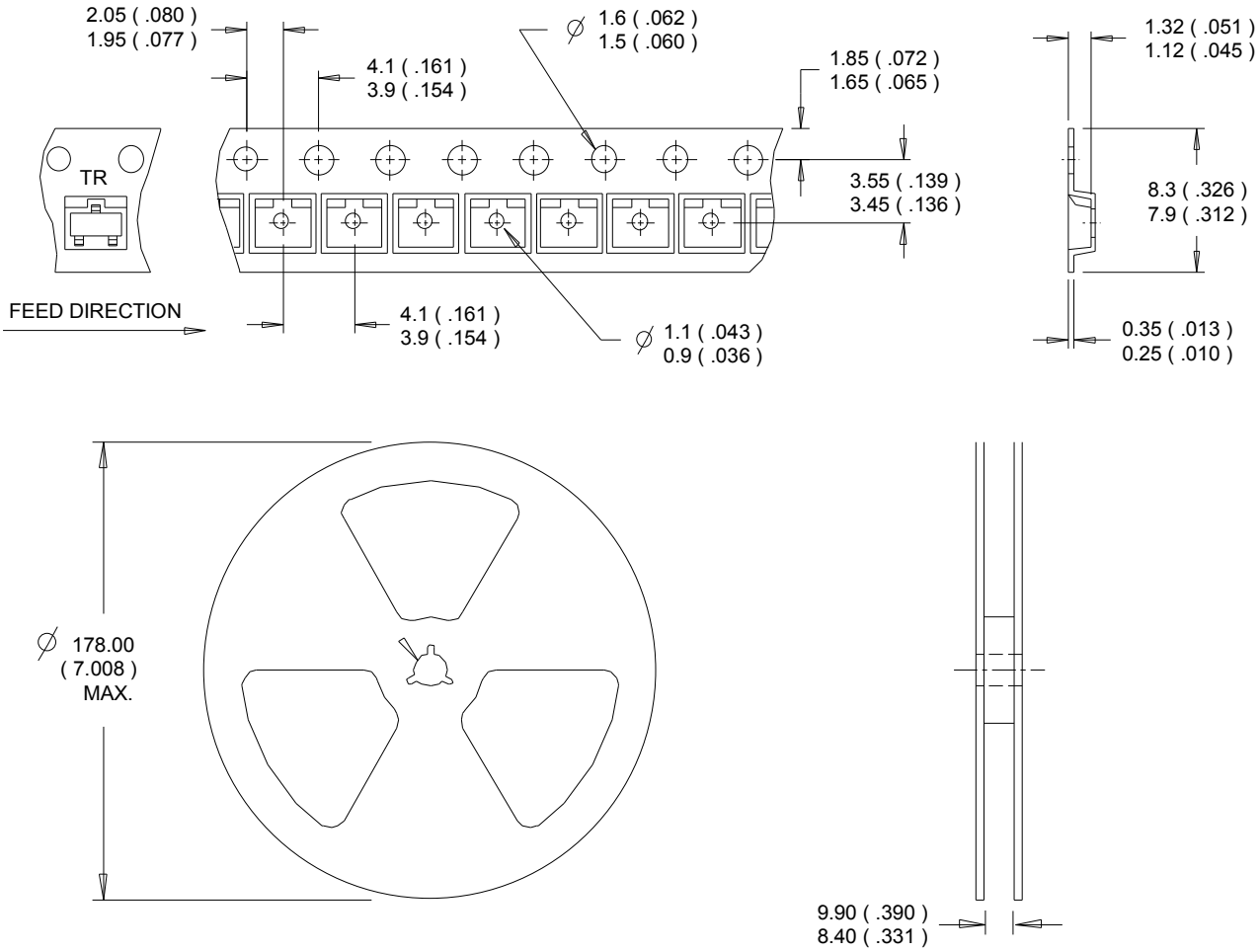
YEAR		Y	WORK WEEK	W
2011	2001	1	01	A
2012	2002	2	02	B
2013	2003	3	03	C
2014	2004	4	04	D
2015	2005	5		
2016	2006	6		
2017	2007	7		
2018	2008	8		
2019	2009	9		
2020	2010	0	24	X
			25	Y
			26	Z

WW = (27-52) IF PRECEDED BY A LETTER

YEAR		Y	WORK WEEK	W
2011	2001	A	27	A
2012	2002	B	28	B
2013	2003	C	29	C
2014	2004	D	30	D
2015	2005	E		
2016	2006	F		
2017	2007	G		
2018	2008	H		
2019	2009	J		
2020	2010	K	50	X
			51	Y
			52	Z

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Micro3™ Tape & Reel Information (Dimensions are shown in millimeters (inches))



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Qualification Information

Qualification Level	Consumer (per JEDEC JESD47F) †	
Moisture Sensitivity Level	Micro3™ (SOT-23)	MSL1 (per JEDEC J-STD-020D) †
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
12/20/16	• Changed datasheet with Infineon logo - all pages. • Removed typo “Industrial” on Feature and Benefits Table on page1. • Corrected typo for Igss test condition from “V_{GS} = 20V” to “V_{GS} = 16V” on page 2.

Edition 2016-04-19
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email: erratum@infineon.com

Document reference
ifx1