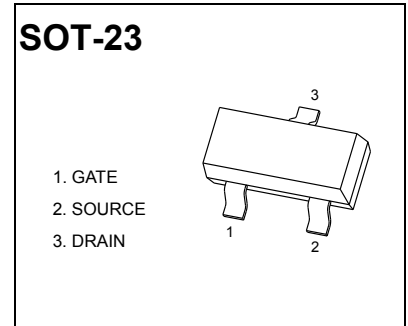


## SOT-23 Plastic-Encapsulate MOSFETS

### 50V N-Channel Enhancement Mode MOSFET

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_D$
50V	0.9Ω@10V	500mA
	1.1Ω@4.5V	



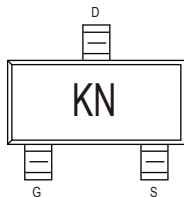
### FEATURE

- High density cell design for low  $R_{DS(ON)}$
- Rugged and Reliable
- Voltage controlled small signal switch
- High saturation current capability
- HMB ESD protected (2000V)

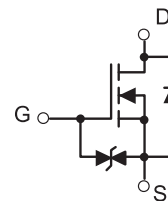
### APPLICATION

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

### MARKING



### Equivalent circuit



### PACKAGE SPECIFICATIONS

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	QTY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	178	3000	203×203×195	45000	438×438×220	180000

### MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	50	V	
Gate-Source Voltage	$V_{GS}$	±12		
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	0.5	A
		$T_A=70^\circ\text{C}$	0.4	
Maximum Power Dissipation <sup>2)</sup>	$P_D$	$T_A=25^\circ\text{C}$	0.3	W
		$T_A=70^\circ\text{C}$	0.2	
Pulsed Drain Current <sup>1)</sup>	$I_{DM}$	1.8	A	
Operating Junction and Storage Temperature Range	$T_J$	150	°C	
Storage Temperature Range	$T_{stg}$	-50 to 150	°C	
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	400	°C/W	

#### Notes

- 1) Pulse width limited by maximum junction temperature.  
2) Surface Mounted on FR4 Board,  $t \leq 5$  sec.

The above data are for reference only.

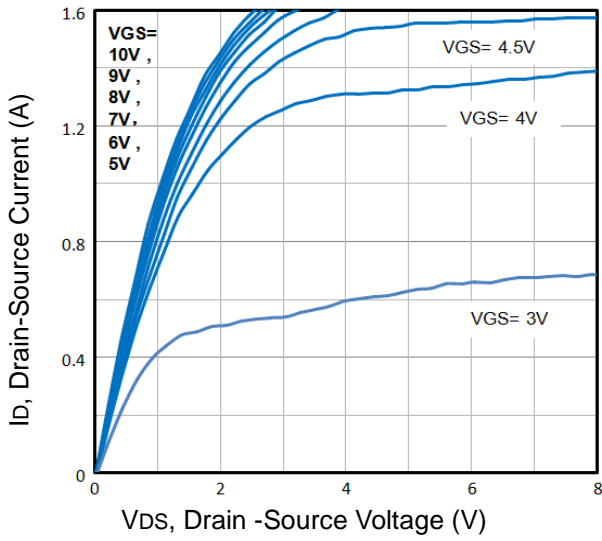
**MOSFET ELECTRICAL CHARACTERISTICS**
 **$T_a=25^\circ\text{C}$  unless otherwise specified**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D=250\mu A$	50			V
Gate-body leakage	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 10$	$\mu A$
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 50V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 40V, V_{GS} = 0V$			100	$\mu A$
<b>On characteristics</b>						
Gate-threshold voltage (note 1)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.60	1.0	1.5	V
Static drain-source on-resistance (note 1)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 0.5A$		0.9	2	$\Omega$
		$V_{GS} = 4.5V, I_D = 0.3A$		1.1	2.5	
		$V_{GS} = 3.3V, I_D = 0.2A$		1.5	4	
Forward transconductance (note 1)	$g_{FS}$	$V_{DS} = 10V, I_D = 0.25A$	100			mS
<b>Dynamic characteristics (note 2)</b>						
Total Gate C harge	$Q_g$	$V_{DS} = 30V, I_D = 0.5A, V_{GS} = 10V$		0.93		nC
Gate-Source Charge	$Q_{gs}$			0.18		
Gate-Drain Charge	$Q_{gd}$			0.31		
Input capacitance	$C_{iss}$	$V_{DS} = 30V, V_{GS} = 0V, f = 1MHz$		23.8		pF
Output capacitance	$C_{oss}$			3.9		
Reverse transfer capacitance	$C_{rss}$			1.5		
<b>Switching characteristics</b>						
Turn-on delay time (note 1,2)	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $I_D = 0.3A, R_{GEN}=3.3\Omega$		6		ns
Rise time (note 1,2)	$t_r$			3.5		
Turn-off delay time (note 1,2)	$t_{d(off)}$			20		
Fall time (note 1,2)	$t_f$			5.9		
<b>Drain-source body diode characteristics</b>						
Source drain current(Body Diode)	$I_{SD}$				0.2	A
Body diode forward voltage (note 1)	$V_{SD}$	$I_S=0.5A, V_{GS} = 0V$		0.78	1.2	V

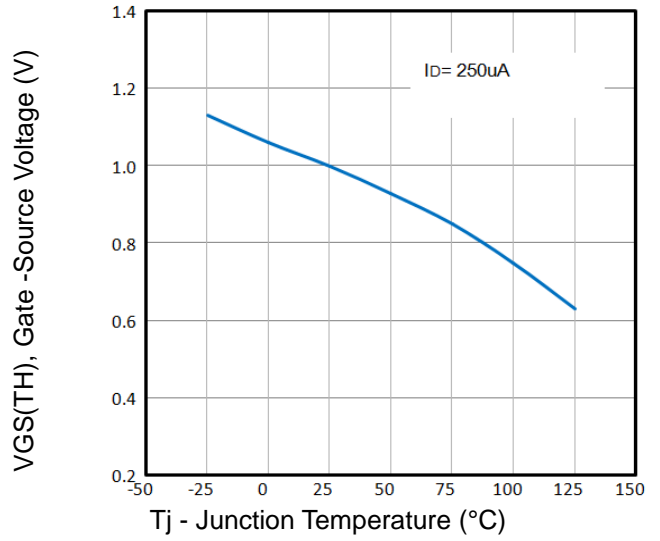
**Notes :**

1. Pulse Test : Pulse Width  $\leq 300\mu s$ , Duty Cycle 2%.
2. These parameters have no way to verify.

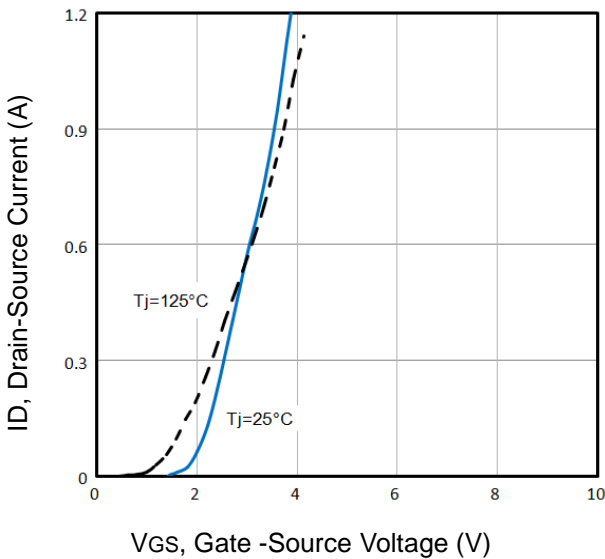
## Typical Characteristics



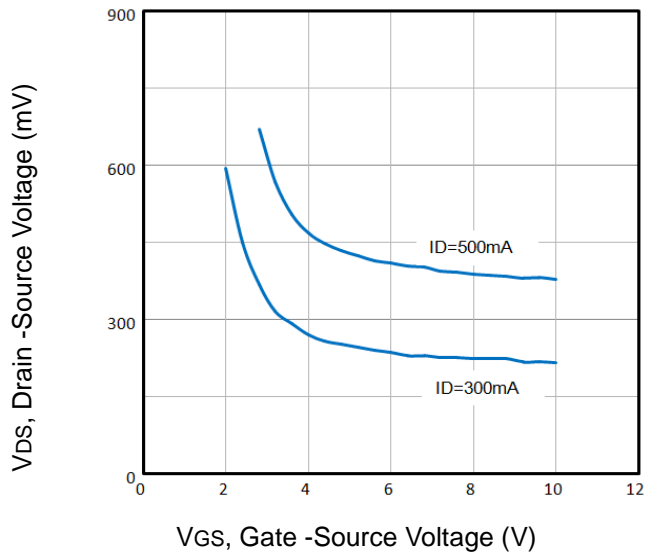
**Fig1.** Typical Output Characteristics



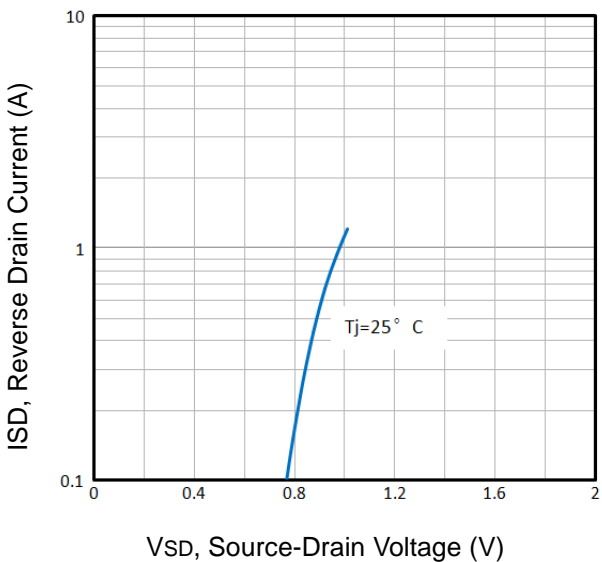
**Fig2.** Normalized Threshold Voltage Vs. Temperature



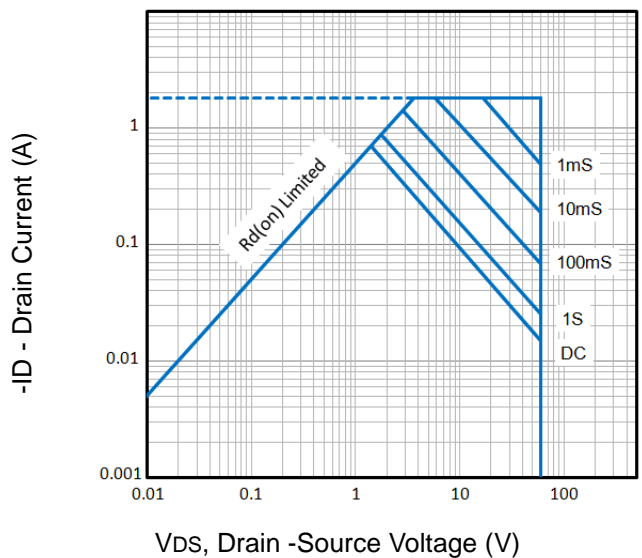
**Fig3.** Typical Transfer Characteristics



**Fig4.** Drain-Source Voltage vs Gate-Source Voltage



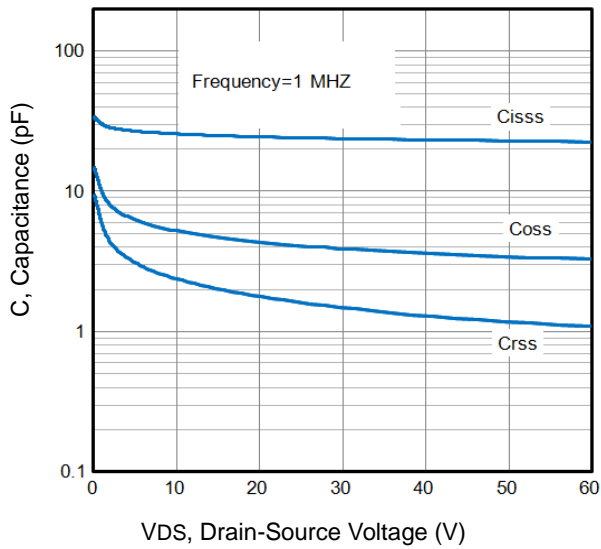
**Fig5.** Typical Source-Drain Diode Forward Voltage



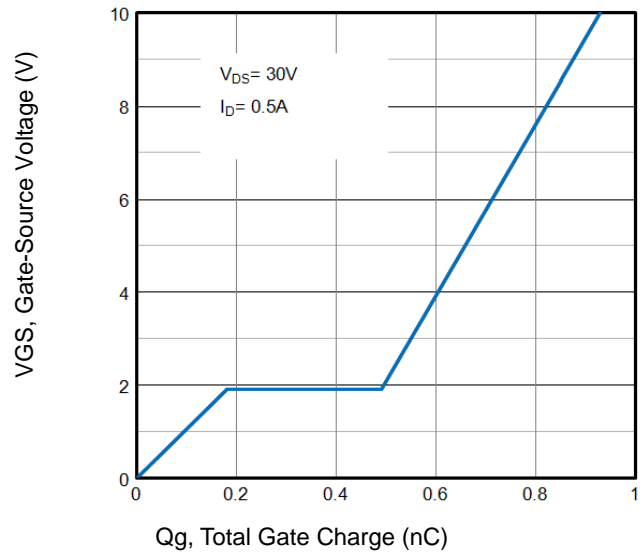
**Fig6.** Maximum Safe Operating Area

The curve above is for reference only.

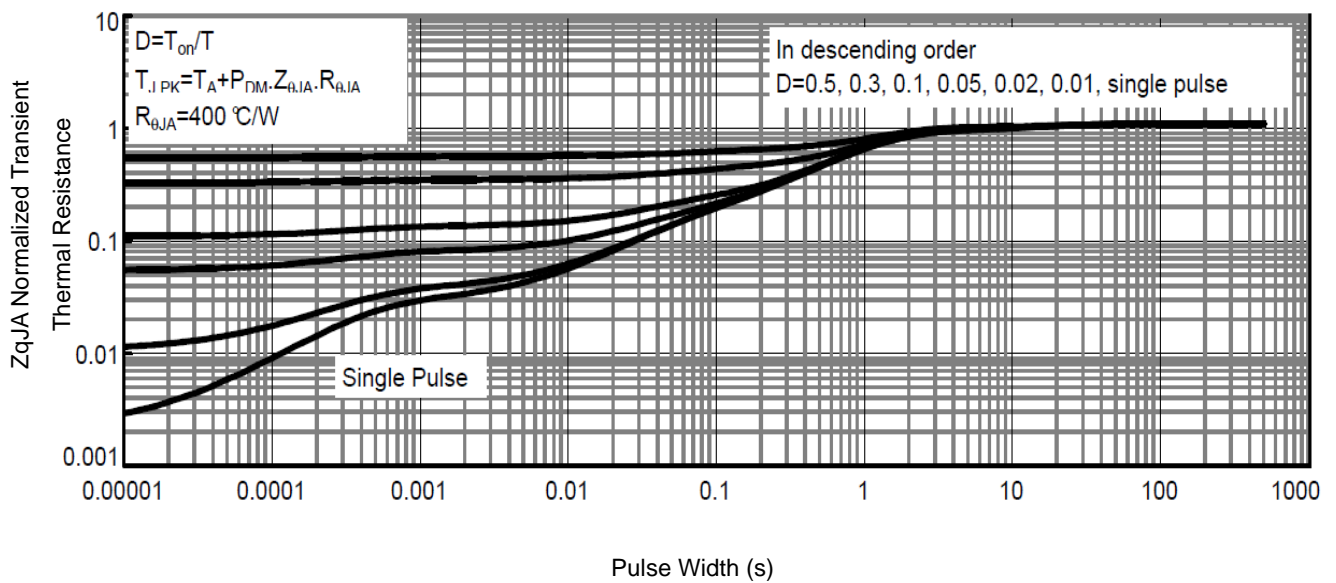
## Typical Characteristics



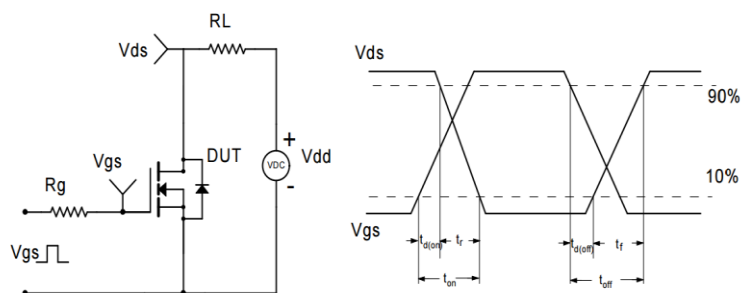
**Fig7.** Typical Capacitance Vs. Drain-Source Voltage



**Fig8.** Typical Gate Charge Vs. Gate-Source Voltage



**Fig9.** Normalized Maximum Transient Thermal Impedance

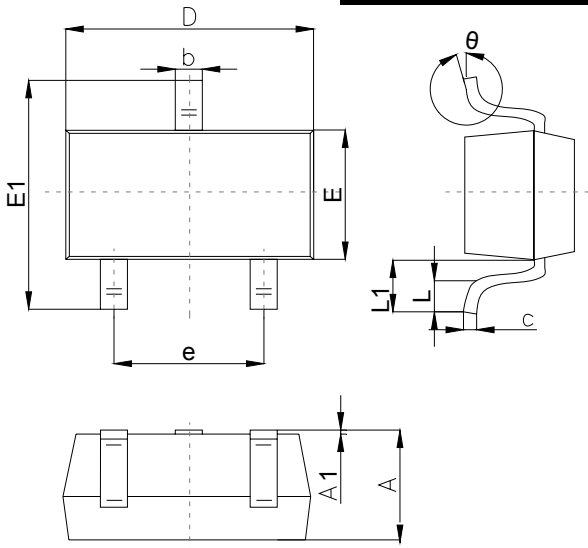


**Fig10.** Switching Time Test Circuit and waveforms

The curve above is for reference only.

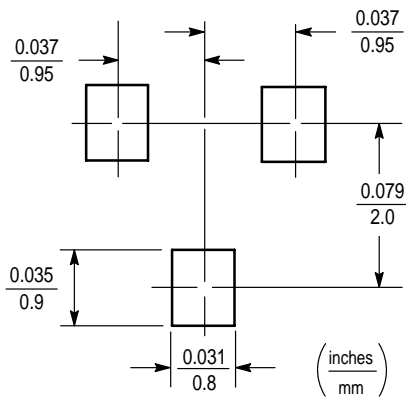
## Outline Drawing

### SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	1.00		1.40
A1			0.10
b	0.35		0.50
c	0.10		0.20
D	2.70	2.90	3.10
E	1.40		1.60
E1	2.4		2.80
e		1.90	
L	0.10		0.30
L1	0.4		
θ	0°		10°

### Suggested Pad Layout



#### Note:

1. Controlling dimension: in/millimeters.
2. General tolerance:  $\pm 0.05$ mm.
3. The pad layout is for reference purposes only.